APPLICATIONS OF INSULATED GATE TRANSISTORS

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ABSTRACT

The ratings and characteristics of the Insulated Gate Transistor, as well as some typical applications of the device, are discussed in this paper. It is a device that features input characteristics similar to a Power MOSFET and output characteristics similar to a bipolar transistor.

INTRODUCTION

The Insulated Gate Transistor (hereafter referred to as the IGT) was designed with an objective of combining the best features of Power MOS and bipolar transistor technologies to produce a device which would approach the ideal switch.

THE POWER MOSFET AND BIPOLAR TRANSISTOR

The Power MOSFET features very fast switching speeds, excellent Safe Operating Areas, and a high input impedance. However, the $R_{DS(ON)}$ of the Power MOSFET increases exponentially with increasing drain-to-source breakdown voltage ratings (i.e., $R_{DS(ON)} = K\ V_{DS}$ exp 2.5 to 2.7) and exhibits a positive temperature coefficient which causes $R_{DS(ON)}$ to more than double from $T_J = 25^{\circ}C$ to $150^{\circ}C$. For devices rated below 100 Volts, the $R_{DS(ON)}$ consists primarily of the channel resistance and a reasonable current rating can be achieved for a given die size. The temperature coefficient of $R_{DS(ON)}$ for devices rated below 100 Volts can be limited to $\Delta R_{DS(ON)} = .2$ to $.7\%/^{\circ}C$. However, as the drain-to-source breakdown voltage is increased beyond 100 Volts, the temperature coefficient of $R_{DS(ON)}$ increases due to $R_{DS(ON)}$ being limited by the channel resistance and the epitaxial resistance - that is, $R_{DS(ON)} = R_{epi} + R_{ch}$. The temperature coefficient of $R_{DS(ON)}$ is not readily reduced for drain-to-source breakdown voltages greater than 100 Volts and is equal to $\Delta R_{DS(ON)} = .6$ to $.7\%/^{\circ}C$. That is, Power MOSFETS have a practical upper voltage limit on BV_{DSS} for a given chip size and current rating which is determined by achievable on-state resistance.

The bipolar transistor features low on-state losses, moderate to very fast switching speeds-depending on voltage and current ratings, as well as drive conditions. However, the bipolar transistor is difficult to drive in applications where optimal switching speeds and low saturation voltages are required, and the drive circuit is generally more complex than a comparable Power MOSFET. The current gain of the bipolar transistor generally decreases as the collector-to-emitter voltage breakdown rating increases, even though very fast switching speeds can be realized. In order to achieve high current gain in bipolar transistors, the Darlington configuration is utilized. However, the on-state losses increase due to the cascade connection of multiple devices. The Safe Operating Areas and peak current capability of the bipolar is generally inferior to Power MOSFETs with comparable voltage and current ratings.

THE IGT

The IGT utilizes the best features of the Power MOSFET and the bipolar transistor. It has a high impedance input with low equivalent input capacitance, as little as one-fifth that of a Power MOSFET rated at comparable voltage and current. The current density of an IGT rated at 400 Volts and 10 Amps is up to twenty times greater than a Power MOSFET and five times greater than a bipolar transistor with comparable ratings. It is a voltage controlled device whose collector-to-emitter saturation voltage can be decreased by increasing gate-to-emitter voltage and resembles the $V_{CE(SAT)}$ characteristics of a bipolar transistor. Switching speeds consist of turn-on times which are comparable to a Power MOSFET, while delay and fall times are controlled by external circuitry and device type.

The symbol and simplified equivalent circuit of the IGT with a resistive load is shown in Figure 1. Q_1 is a MOSFET with a parasitic transistor (Q_2) whose base-to-emitter junction has connected in parallel with it a low value of resistance R1. R1 is shown as a variable resistor. This is due to process variations and different geometric locations of the multiple cells which are present in a large device. R2 is an equivalent resistance used to describe (in simplistic terms) a functional realization of a Power MOSFET whose channel and epitaxial resistance are modulated to provide an equivalent $R_{DS(ON)}$ much lower than a comparably rated Power MOSFET. C1 is collector-to-base capacitance of the parasitic transistor Q_2. Q_2 does not conduct at rated

(a) Symbol

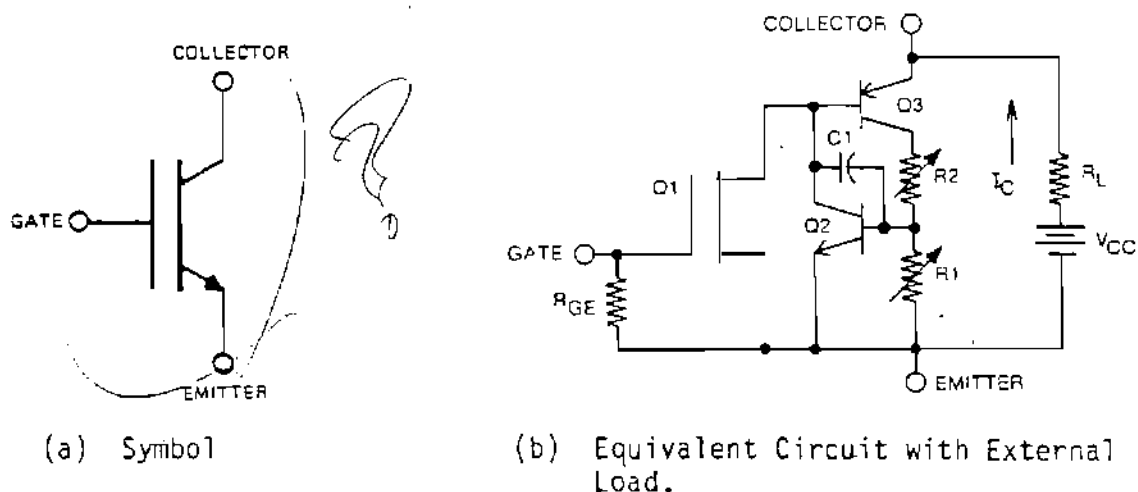(b) Equivalent Circuit with External Load.

FIGURE 1 - IGT Symbol and Equivalent Circuit.

values of IGT collector current and maximum junction temperature when the device is forward biased.

In order to turn the IGT on, Q_1 gate-to-emitter must be biased positive to negative. When $V_{GE(th)}$ is exceeded, load current flows through Q_3 base-to-emitter junction and through Q_1 drain-to-source. This current through Q_1 initiates the turn-on sequence. That is, Q_1 conducts until the turn-on delay time (t_{d1}) of Q_3 is exceeded. After time t_{d1}, the value of R2 changes drastically to lower the effective on-state voltage from collector-to-emitter of the IGT. That is, $V_{CE(Q3)} + I_{CQ3} \cdot R2 = V_{BE(Q3)} + I_{D(Q1)} \cdot R_{DS(ON)Q1}$ - where $R_{DS(ON)}$ is effectively in parallel with the dynamic "on" state resistance R2. Q_3 is a low gain device and $V_{CE(SAT)} \cong V_{BE}$. R1 is important to the device design, since it must be properly sized to avoid latch-up of the parasitic SCR consisting of Q_2 and Q_3 at extreme current levels and/or junction temperatures.

In order to turn the IGT off, the gate-to-emitter voltage is reduced to zero. This turns Q_1 off, decreases the base and collector currents of Q_2 and starts the turn-off sequence. The collector current fall time will consist of three distinct intervals - turn-off delay time [$t_{d(OFF)}$], current fall time one (t_{f1}) and current fall time two (t_{f2}). The turn-off delay time will be influenced by the value of R_{GE} and the magnitude of V_{GE} prior to turn-off, as well as the storage time of Q_3. Since there are no means of extracting charge from Q_3, the turn-off delay time and fall time is controlled by the individual device characteristic. Therefore, the current fall time will consist of two distinct intervals (t_{f1} and t_{f2}). A current tailing effect will be evident and will not be controllable by the external circuitry, since the PNP (Q_3) must turn off by recombination.

LATCHING CURRENT

The IGT can latch on during turn-off due to the parasitic SCR (Q_2 and Q_3) if the value of gate-to-emitter resistance is too small. Typical device switching times and controllable collector currents are specified with a minimum permissible value of gate-to-emitter resistance. It must be emphasized that latching generally occurs during device turn-off. Referring to Figure 1, it is observed that in the forward conducting mode of the IGT with R_{GE} fixed, an increase in the magnitude of the collector current beyond rated values will result in a corresponding increase of $V_{CE(SAT)}$. This effectively increases the applied voltage to the collectors and emitters of Q_2 and Q_3. It is well known that increasing V_{CE} increases the relative current gain of bipolar transistors when in the quasi saturated region, and if the junction temperature is increased, the gain also increases. An exception to this is when the magnitude of the collector current is much greater than rated current and current crowding effects (gain roll off) cause very low gains.

The IGT is very difficult to latch on in the forward conducting mode due to R1 - which is a very low value of resistance. However, it is much easier to latch on while turning off the device. During turn-off of the IGT, R_{GE} determines the turn-off dV_{DS}/dt of the Power MOSFET (Q_1). The dV_{DS}/dt of Q_1 equals the dV_{CE}/dt of Q_2. Due to capacitive charging currents which are developed across R1, it is possible to initiate Q_2 conduction due to excessively high values of dV_{CE}/dt. The PNP transistor (Q_3) also experiences a gain in-

crease due to its V_{CE} increasing, since the emitter potential of Q_3 is one diode drop greater than $V_{CE(Q1)}$.

Since the gain of Q_2 and Q_3 increase as a function of temperature and the magnitude of collector-to-emitter voltage, the predicted behavior is that latching current will be high at 25°C and decrease as a function of increasing junction temperature and increased dV_{DS}/dt of Q_1 (minimum R_{GE}). It will also be higher for a resistive load than a clamped inductive load – since maximum dV/dt occurs at maximum current. Experimental results, as well as production testing, confirm these hypotheses. Typical latching currents are shown as a function of temperature for a 10 Amp IGT rated at 400 VDC in Figure 2.
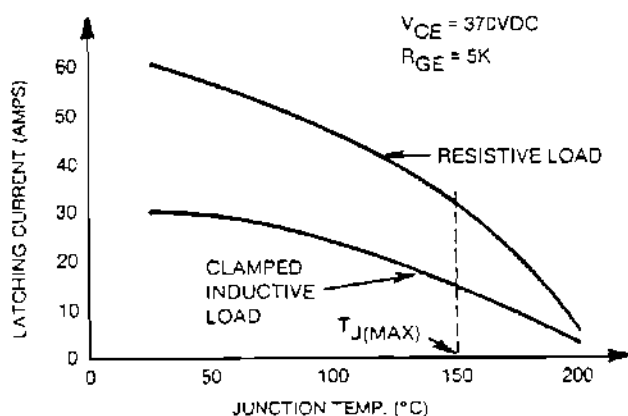
FIGURE 2 - Typical Latching Current vs. Junction Temperature.

In practical devices, the current fall times are controlled by tailoring individual device characteristics for gain and switching speeds. Devices have been successfully constructed with fall times that vary from as low as 200 ns up to 30 µs maximum. The fast turn-off times are achieved at the expense of increasing collector-to-emitter saturation voltage. This is illustrated in Figure 3. It is observed that very fast devices (type A) have high forward voltage drops at rated current, moderately fast devices (type B) compare favorably with power Darlingtons for $V_{CE(SAT)}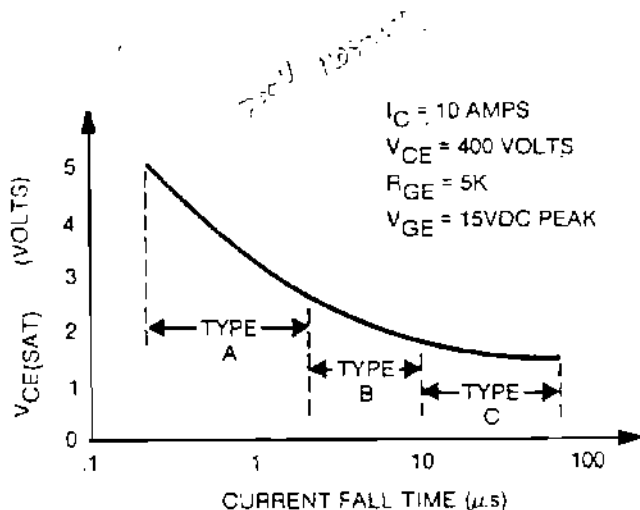$ while type C devices can be fabricated to have $V_{CE(SAT)}$ values equal to or less than a comparably rated power Darlington.

FIGURE 3 - $V_{CE(SAT)}$ vs. Current Fall Time ($t_{f1} + t_{f2}$).

TEMPERATURE COEFFICIENTS OF THE IGT

The temperature coefficients of the IGT are shown in Figure 4. It is observed that BV_{CER} has a positive temperature coefficient and is approximately + .117%/°C. In a typical application, the lowest operating temperature should be used to determine device specifications. For example, a 400 Volt device would be rated at 349 Volts at T_J = -50°C and 451 Volts at T_J = 100°C.

The gate-to-emitter threshold voltage has a negative temperature coefficient of approximately -6.7 mV/°C. In practical applications,

the maximum operating junction temperature should be considered for minimum noise immunity, while the minimum junction temperature should be considered for maximum $V_{GE(th)}$ in order to determine minimum values of the gate-to-emitter drive requirements. That is, for T_J = 25°C, $V_{GE(th)}$ = 3.5 VDC, while at T_J = 150°C, $V_{GE(th)} \cong$ 2.3 VDC. Noise voltages in excess of this value could turn the device on. At T_J = -50°C, $V_{GE(th)}$ is = 4.18 VDC and represents the minimum value of $V_{GE(th)}$ that could be applied to the device. In a switched mode application, the gate-to-emitter voltage is >> $V_{GE(th)}$ in order to minimize $V_{CE(SAT)}$ and reduce conduction losses. In linear and parallel applications, $V_{GE(th)}$ becomes important in order to predict circuit performance - this is similar to Power MOSFET design procedures.
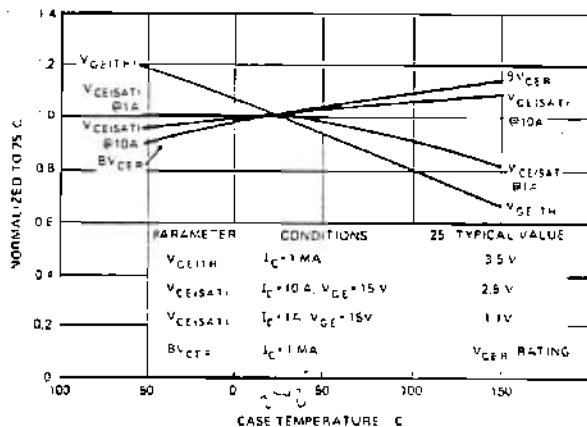
FIGURE 4 - Typical Temperature
           Dependence of Parameters.

The temperature coefficient of $V_{CE(SAT)}$ for the IGT is a parameter that provides an indication of just how well the IGT overcomes the shortcomings of Power MOSFETs and bipolar transistors. That is, Power MOSFETs are easily paralleled for D.C. applications due to the positive temperature coefficient of $R_{DS(ON)}$. However, for pulsed type loads, the Power MOSFET should be matched for transconductance and gate-to-source threshold voltage to assure proper dynamic balance.

The bipolar transistor is not as easy to parallel, since the temperature coefficient is negative. Ballast resistors can be added externally to the device to improve current sharing for absolute magnitudes of collector current. However, pulsed applications present a problem when high speed switching is required. Considerable effort must be expended by the circuit designer to achieve effective paralleling. This includes matching transconductance, gains, switching times, and use of bucking inductors. In addition, optimal drive techniques must be employed in order to assure simultaneous switching of the devices during turn-on and turn-off.

The IGT has a temperature coefficient of $V_{CE(SAT)}$ that looks like a bipolar transistor up to approximately $I_{C(MAX)}/2$. At that point, the temperature coefficient becomes zero. At collector currents greater than $I_{C(MAX)}/2$, the temperature coefficient becomes positive and looks like a Power MOSFET. A typical temperature coefficient of $V_{CE(SAT)}$ as a function of collector current and junction temperature is given in Figure 5. The implications of this are that an IGT can be easily paralleled for d.c. and low frequency applications. High speed pulsed applications would require that differential turn-off times be balanced. Referring to Figure 4, it is observed that the coefficient of $V_{CE(SAT)}$ for -55°C $\leq T_J \leq$ 150°C at 10 Amps collector current is positive and is equal to approximately + .073%/°C. It should also be observed from Figure 5 that the temperature coefficient of $V_{CE(SAT)}$ for a 15 Amp device is zero at approximately $I_C/2$.

In order to appreciate the significance of an IGT rated at 10 amperes and 400 Volts with a zero temperature coefficient for $V_{CE(SAT)}$, consider an equivalent Power MOSFET rated at 400V DC and 10 amperes with identical drive conditions. That is, $V_{GE} = V_{GS} = 10$ Volts for $25 \leq T_J \leq 125^oC$. The General Electric D94FQ4 has an on-state voltage of 2.5 Volts typical and 2.7 Volts maximum at $T_J = 25^oC$. Assuming a temperature coefficient of .073%/^oC, $V_{CE(SAT)}$ max. at $T_J = 125^oC$ is 2.89 Volts. Power dissipation due to conduction losses would be $27 \leq P_D \leq$ 29 Watts for $25 \leq T_J \leq 125^oC$.

FIGURE 5 - $V_{CE(SAT)}$ vs. I_C and T_J for a 15 Amp IGT.

An equivalent Power MOSFET, the GE D86EQ2 and IRF340 lists $R_{DS(ON)} = .55$ Ohms max. at $T_J = 25^oC$. Using the t.c. of $R_{DS(ON)} \cong .6$ to $.7\%/^oC$ gives a 60% change in $R_{DS(ON)}$. That is $R_{DS(ON)}$ max. will be .88 Ohms and $V_{DS(ON)}$ will be 8.8 Volts with $P_D = 88$ Watts at $T_J = 125^oC$. That is, the IGT on-state losses are approximately one-third the Power MOSFET.

This implies that the IGT is a much better device for d.c. and low frequency applications at high voltages ($V_{CE} \geq 400$ VDC). This does not imply that the IGT is the best device for all applications, since the Power MOSFET is vastly superior to the IGT for high frequency pulsed type applications where switching losses exceed conduction losses by a considerable margin.

Consider the situation where an IGT type A (Figure 3) has a current fall time of 350 ns at $T_{J(MAX)} = 125^oC$ and is switching an inductive load at 100 kHz. The total losses will consist of conduction losses and switching losses. That is, for the IGT,

$$P_T = V_{CE(SAT)} I_C (\delta) + \frac{V_{CC} I_C f t_f}{2}$$

where δ = duty cycle = .5 and $f = 10^5$ Hz

let $I_C = 10$ Amps and $V_{CC} = 400$ VDC, $V_{CE(SAT)} = 5$ VDC (from Figure 3)

then $P_T = 25 + \frac{4(10^3) \ (10^5) \ .35 \ (10^{-6})}{2} = 95$ Watts

An equivalent Power MOSFET would have a fall time of approximately 50 ns. Therefore, $P_D = 44 + 10 = 54$ Watts (from previous example) for the Power MOSFET. The Power MOSFET is clearly the device to choose in order to minimize power losses at $f = 100$ kHz. The question naturally arises as to "when should one use an IGT or a MOSFET?" In order to answer this, equate total losses and solve for frequency. That is, for this example, the fre-
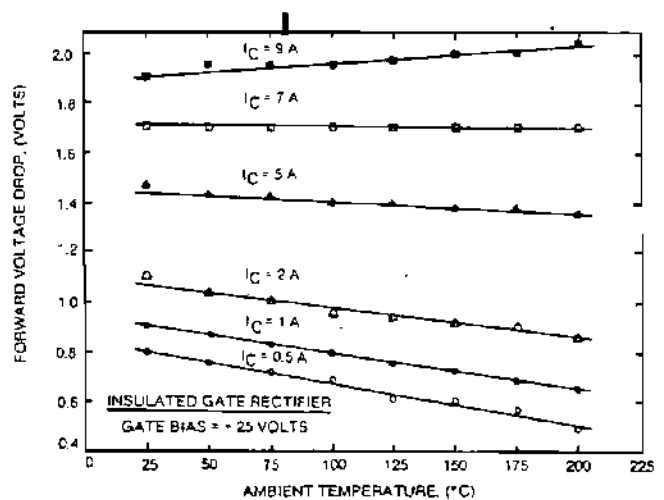
quency crossover point would be at f = 41.42 kHz.

The bipolar transistor can certainly function at 40 kHz and also at 100 kHz quite efficiently. However, drive circuit complexity far exceeds that which which is required for a Power MOSFET or IGT in order to achieve optimal switching times. In addition, switching times of the Power MOSFET are virtually constant over wide junction temperature excursions as well as dynamic load changes.

D.C. and low frequency applications minimize the significance of switching times but maximize the importance of low conduction losses. This is where IGT type C (Figure 3) comes into the picture. The conduction losses of a 400 Volt IGT are equal to or less than an equivalent bipolar and the IGT is easily paralleled to increase its current ratings. Bipolar transistors are well suited for these applications, but the resultant gate drive simplicity of an IGT compared to bipolar drive circuits results in equivalent performance with extremely simple gate-to-emitter drive circuitry due to its high input impedance.

SWITCHING THE IGT

The IGT switching times are composed of turn-on delay time [$t_{d(ON)}$] , rise time (t_r), turn-off delay time [$t_{d(OFF)}$] and fall times (t_{f1} and t_{f2}). The turn-on delay and rise times are similar to a Power MOSFET and are a function of the source impedance and source voltage. Typical values for the GE D94FQ4, 400 Volt 10 Amp device are 100 and 120 ns, respectively, for $t_{d(ON)}$ and t_r with a 15 Volt source voltage and a 50 ohm source impedance at T_J = 150°C.

The turn-off time of the IGT depends on the value of the gate-to-emitter voltage prior to turn-off and the gate-to-emitter source impedance. Turn-off times are specified on the data sheet with a minimum permissible value of 1K for R_{GE} and a typical value of R_{GE} = 10K with a gate-to-emitter voltage of 15 Volts. Turn-off delay times for a resistive load are 11 and 2.5 µs maximum for R_{GE} = 10K and 1K, respectively at T_J = 150°C. Fall times are specified as 6 and 2 µs for R_{GE} = 10K and 1K, respectively, at T_J = 150°C for a resistive load. Clamped inductive switching times are specified at T_J = 150°C, V_{CE} = 400 Volts, I_C = 10 Amps, V_{GE} = 15 Volts, with R_{GE} = 10K and 1K. $t_{D(OFF)}$ is 16 and 3.6 µs, t_f is 4.4 and 1.7 µs, respectively, for R_{GE} = 10K and 1K.

It was mentioned earlier that the IGT has a current tail that is independent of the drive circuitry. Figure 6 is a plot of turn-off times vs. R_{GE} for a resistive load. The current tail (t_{f2}) is observed to be a constant at a fixed temperature. The effects of the tail contribute to switching losses for a resistive and inductive load during turn-off. It can be shown by analysis that increased switching losses due to t_{f2} compared to devices with a linear fall time are such that at f = 10 kHz for a type B device (the GE D94FQ4) operating at 10 kHz, 400 Volts, 10 Amps with t_{f1} = .5(10^{-6}) and t_{f2} = 2(10^{-6}), the resistive switching losses are 10.72 Watts compared to a device with linear fall time whose switching losses would be 7 Watts. The switching losses for an inductive load would be 25 Watts for the IGT and 21 Watts for a device that has linear current fall time.

Figure 7 is a photo of actual device switching times. It should be observed that for a slow device (type C) the tail is quite obvious. This device would be used for d.c. and low frequency applications where switching losses are minimum. A type A device switches so fast that the current tail is hardly noticed.

OUTPUT CHARACTERISTICS AND TYPICAL VALUES OF $V_{CE(SAT)}$

The IGT can be used as a linear amplifier or in the switched mode. In the switched mode, increasing the magnitude of V_{GE} decreases $V_{CE(SAT)}$. In addition, for constant V_{GE} (7 Amps for example) the device acts as a current source and self limits its collector current. Sufficient heat sinking must
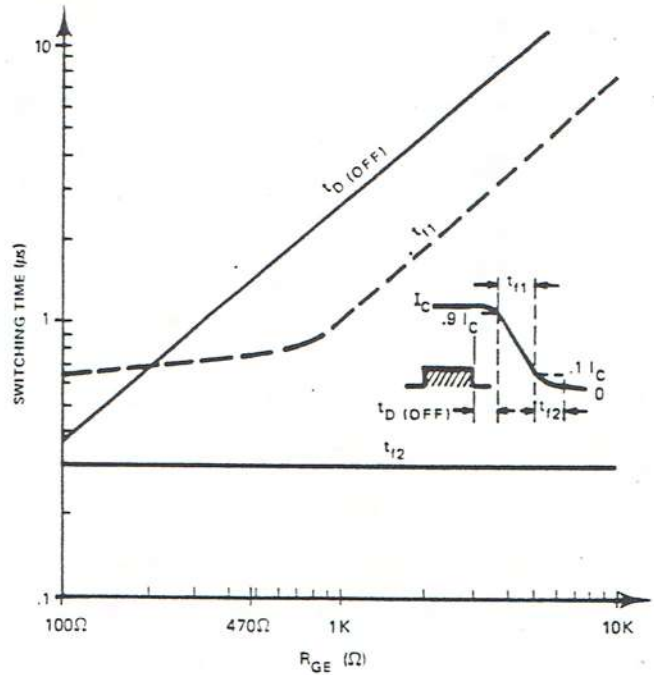
FIGURE 6 - Turn-off Times vs. R_{GE}.
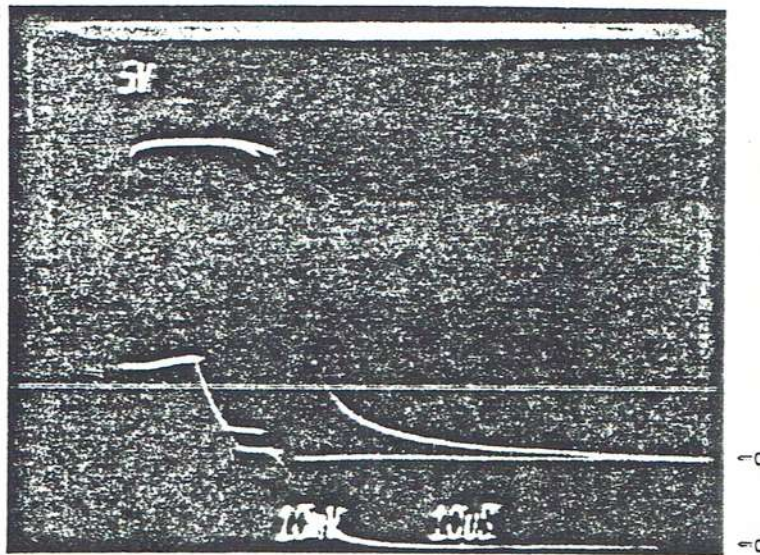
TOP (I_c) VERT=2A/cm BOTTOM (V_{GE}) VERT= 5V/cm

FIGURE 7 - Resistive Load Switching.

be provided to operate the device as a current source.

The on-state characteristics of the D94FQ1FR4 are shown in Figure 9. It is observed that the temperature coefficient is zero at approximately 4 Amps.
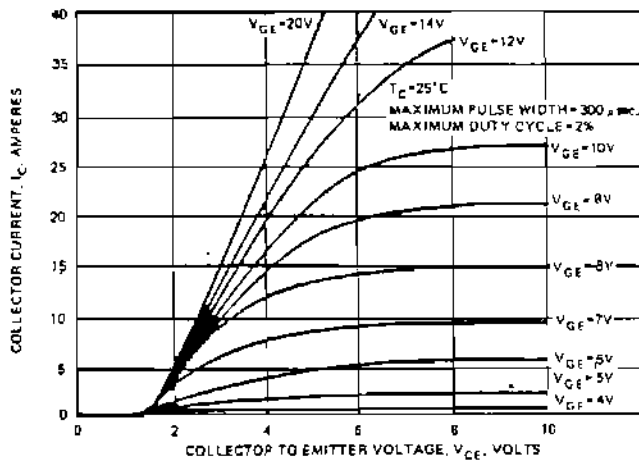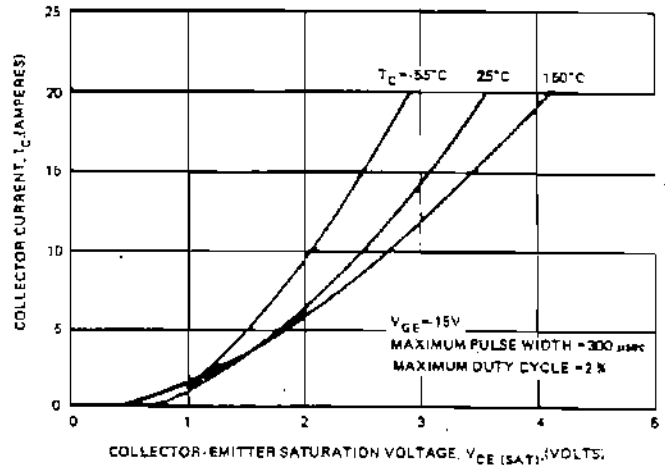
FIGURE 8 - Typical Output
Characteristics.

FIGURE 9 - Typical Collector-
Emitter Saturation
Voltage.

SAFE OPERATING AREAS AND TYPICAL CHARACTERISTICS

Safe Operating Areas for the GE D94FQ/FR4 IGT are shown in Figures 10 thru 12. The maximum value of switched (pulsed) collector current is limited by the minimum value of R_{GE} that can be tolerated without causing the device to latch on due to loss of gate control. In addition, maximum pulsed collector currents are significantly greater than continuous collector current ratings due to the effects of duty cycle, pulse width, and the transient thermal resistance of the device. The maximum Safe Operating Area for the D94FQ/FR4 is shown in Figure
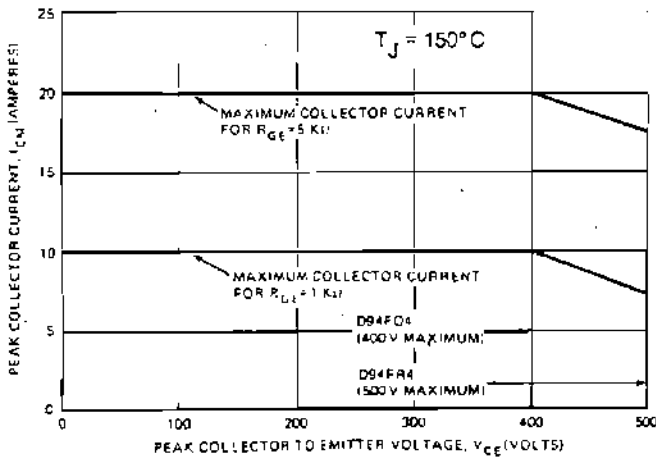
FIGURE 10 - Maximum Rated Switch-
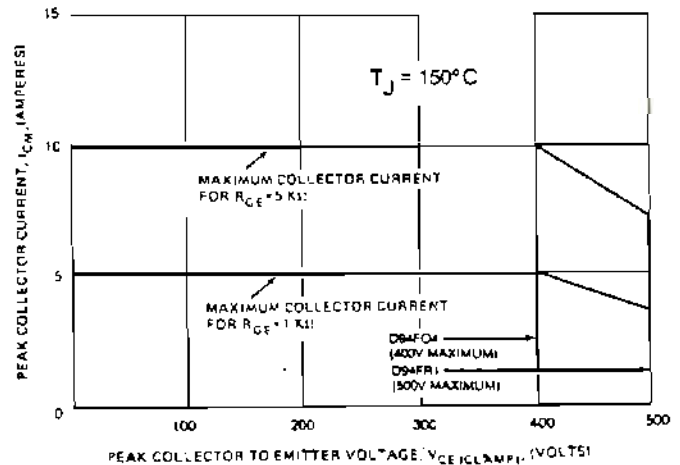ing Safe Operating
Area for Resistive
Load.

FIGURE 11 - Maximum Rated Switch-
ing Safe Operating
Area for Inductive
Load.

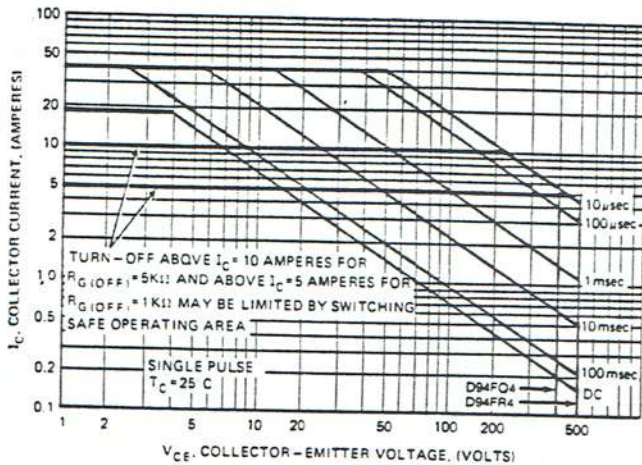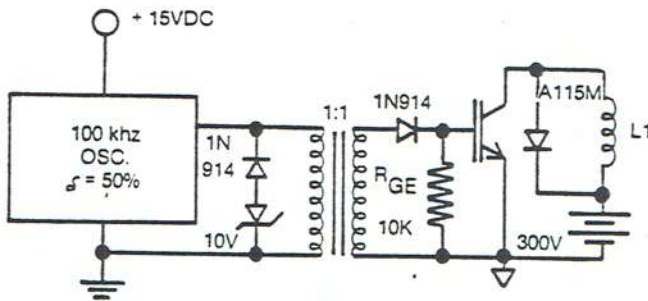12. Note that peak current ratings for a 10 Amp IGT is 40 Amps and that the SOA depends on R_{GE}.

FIGURE 12 - Maximum Safe Operating
Area.

GATE DRIVE

Gate drive circuits for the IGT can be as simple as a voltage source with a gate-to-emitter resistance. Figure 13 is an illustration of several simplified drive circuits. In Figure 13a, the turn-off delay time of the IGT is sufficiently long to allow high frequency pulses to drive the device. That is, select the off time (5 μs) of the oscillator to be less than $t_{d(OFF)}$ to minimize transformer size and drive power. In Figure 13b, a symmetrical drive is utilized to drive an inductive load in a low frequency application. Note that only one resistor is required and that current fall time is sufficiently slow to negate the need for a snubber or voltage clamp. In Figure 13c, an asymmetrical drive is utilized to achieve rapid turn-on time with the fall time being controlled by R_{GE} for a high speed application. In Figure 13d, Q_3 is driven by a current source. The charging current is selected by the value of R_E,
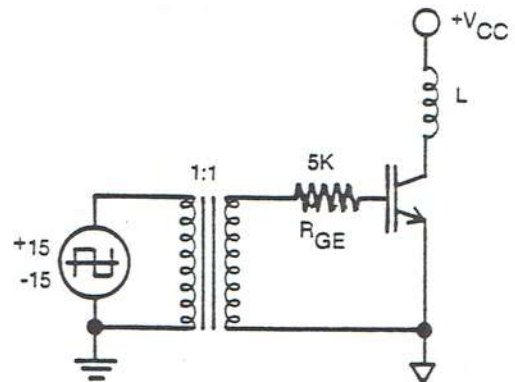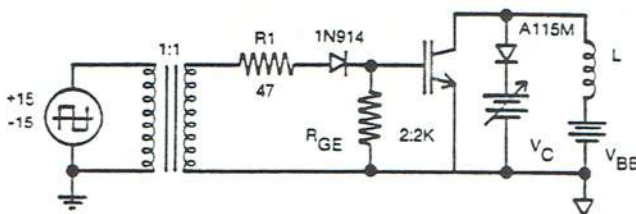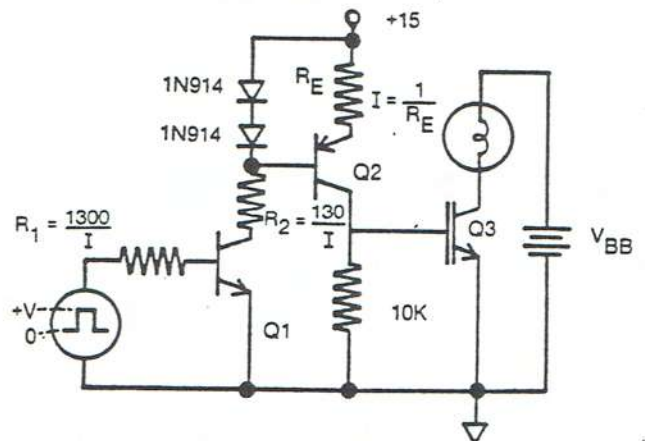
where $I_{Q2} = \dfrac{1}{R_E}$.

13(a) High Frequency Drive for
Solenoid.

13(b) Symmetrical Drive.

13(c) Asymmetrical Drive with
Clamped Inductive Load.

13(d) Current Source Drive.

FIGURE 13 - Gate Drive Circuits.

SUMMARY

The IGT is an exciting and versatile device. It can be tailored to function in low frequency, mid-frequency, and high frequency applications. It is not intended to replace bipolar transistors or Power MOSFETs, but is intended to provide designers with a new device that features improved performance, drive circuit simplicity, and brings to the marketplace a device that combines the best features of bipolar and Power MOSFET technology.