Lecture 30: Cleanroom design and contamination control

Contents

1 Introduction

Yield improvement is the biggest challenge in integrated circuit fabrication. Initially, process is focused on producing a wafer with a *yielding die*, i.e. a die that works according to the IC specification. Once, that has been obtained yield steadily increases. The limiter for yield is usually *wafer contamination* in the fab. This has become even more important now, since device dimensions are currently in the *nm* range. Cleanroom technology is designed to minimize this contamination. Figure 1 shows two examples of particles on wafer. A particle between two metal lines can cause shorting of electrical signals. Figure 2 shows SEM images of two types of defects that have caused

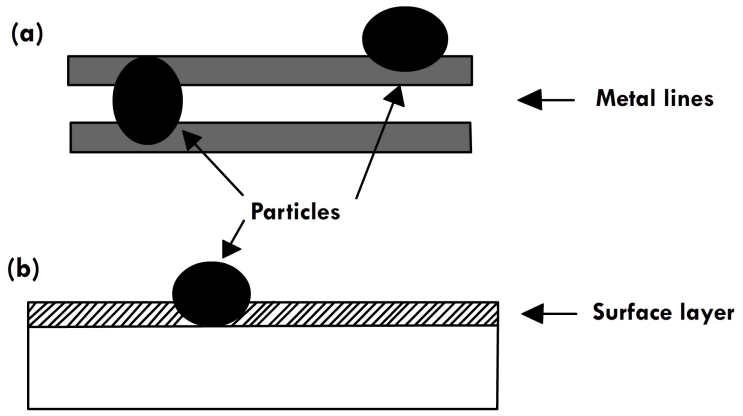


Figure 1: Defects between (a) metal lines and (b) on the surface of a wafer. Surface defects can affect the growth of new layers while defects between metal lines can cause electrical shorts. Adapted from *Microchip fabrication - Peter van Zant.*

an open circuit and a short circuit. Particles on surfaces can cause errors in lithography by interfering with the masking process. As device dimensions shrink, the minimum dimensions of these defect particles also shrink. Some typical sizes of contaminants are shown in figure 3.

2 Contaminant types

Contaminants can be divided into five main classes.

2.1 Particles

Current device dimensions in the semiconductor industry are in the nm range. The devices are also densely packed, so that the spacing between adjacent lines are also in the nm range, see figure 1. Compared to this, human hair is approximately 100 μm in diameter and typical dust particles are 1 μm in size. Some common particle sources in the fab are

1. People working in the fab
2. Generated by fab equipment
3. Processing chemicals

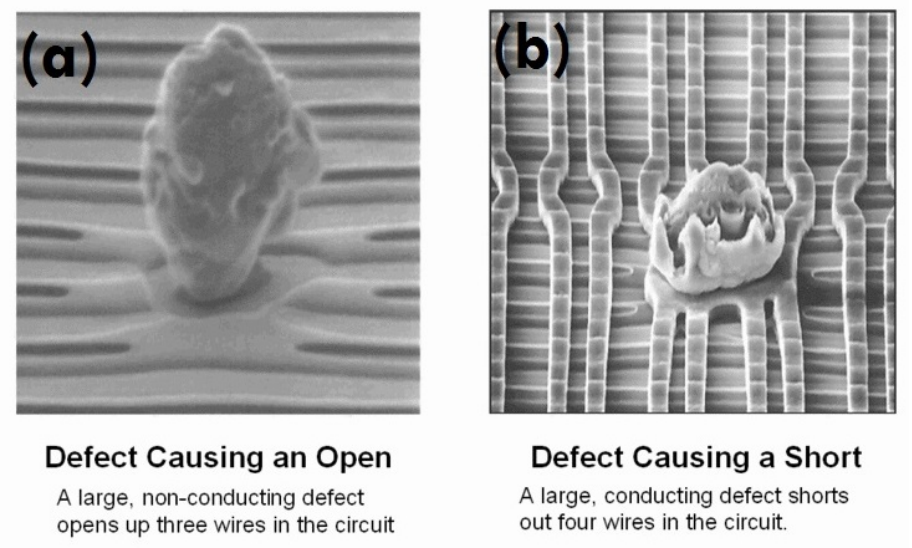


Figure 2: SEM image of defects causing (a) an open circuit and (b) short circuit. In typical integrated circuits, these defects need to be only a few microns wide to affect the electrical signals and as device dimensions shrink the size of these *killer defects* also shrinks. Adapted from *http://www.si2.org/openeda.si2.org/dfmcdictionary/index.php/Random_Defects*

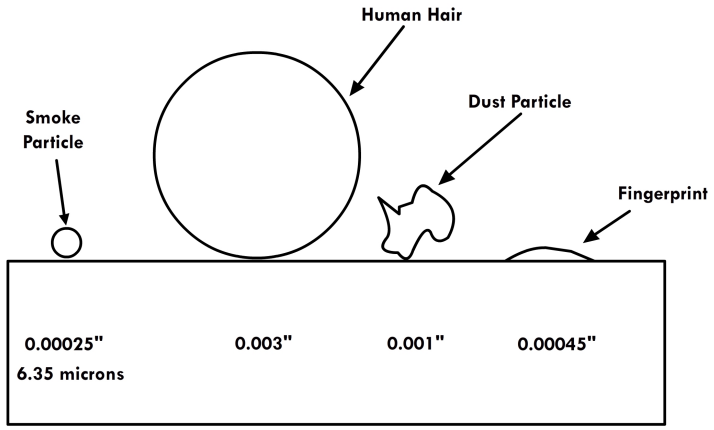


Figure 3: Typical sizes of common contaminants on wafers. These are all related to wafer handling in the fab. To minimize these defects, wafers are exposed to the fab environment only under extremely controlled conditions. Adapted from *Microchip fabrication - Peter van Zant.*

Table 1: Trace impurities in a commonly used resist stripper in the fab. Concentrations are in *ppb*. The data values are sourced from *Microchip fabrication - Peter van Zant.*

Impurity	**Concentration** (*ppb*)
Sodium	50
Potassium	50
Iron	50
Copper	60
Nickel	60
Aluminum	60
Manganese	60
Lead	60
Zinc	60
Chlorides	1000

The rule of thumb for particle contaminants is that the *maximum allowable size must be smaller than one-half the first metal layer half pitch.* With decreasing device dimensions, the ability to detect these small particles becomes important.

2.2 Metal ions

Dopant concentrations in semiconductors are very small, of the order of 10^{15} to 10^{17} ions per cm^{-3} (typically *ppm* or *ppb*). Presence of electrically active impurities or contaminants can alter device performance. These impurities are called *mobile ionic contaminants* (MICs). These are ions that have high mobility in the semiconductor. They can cause failure even after packaging (they might not be detected during sort). Sodium is the most common MIC, which is commonly found in chemical sources. Table 1 shows concentrations of metallic impurities in resist strippers. The MICs can affect the metal oxide semiconductor (MOS) junction by modifying the barrier potential. Special low metal grade chemicals have been developed for use in the semiconductor industry, to overcome this problem.

2.3 Chemicals

Another source of contaminants are unwanted chemicals that contaminate process chemicals and deionized water that are used in various steps in the fabrication process. They can affect the regular processing e.g. contamination in the etchant can cause non uniform etching or change the etching rate.

Chlorine is a common contaminant that is found in these chemicals.
Bacteria is another common contaminant that can grow on unwashed surfaces. These can act as particulate contaminants and also as a source of metallic ions.

2.4 Airborne Molecular contaminants

Airborne molecular contaminants (AMCs) are contaminants from process tools or chemical delivery systems. They enter the fabrication area and cause defects on the wafers. AMCs can be gases, dopants, process chemicals, moisture, and/or organics. A common source of AMCs is during wafer transfer in the in the fab. Wafer transfer and storage usually happens through FOUPs (front opening universal pods). The FOUP is a plastic container with grooves for holding wafers and outgassing of the FOUP can contaminate the wafers. Thus, wafers stored in the fab for long time can pick up dust just by sitting in these FOUPs. One solution is to use nitrogen purged FOUPs to minimize dust particles.

2.5 Contamination problems and sources

The presence of contaminants can cause three major effects

1. **Device yield** - this is the most obvious effect and can be easily be detected. Contaminants can cause the die to fail electrical tests and thus reduce yield.

2. **Device performance** - contamination can cause a lowering of device performance with time. This is a more serious problem because it causes lowering of device life.

3. **Device reliability** - this is the hardest to detect because this can lead to failure in service. Sometimes, it might not even be detected during electrical testing during sort.

The general sources of contamination are

1. Air

2. Fabrication facility

3. Cleanroom personnel

4. Process water, chemicals, and gas

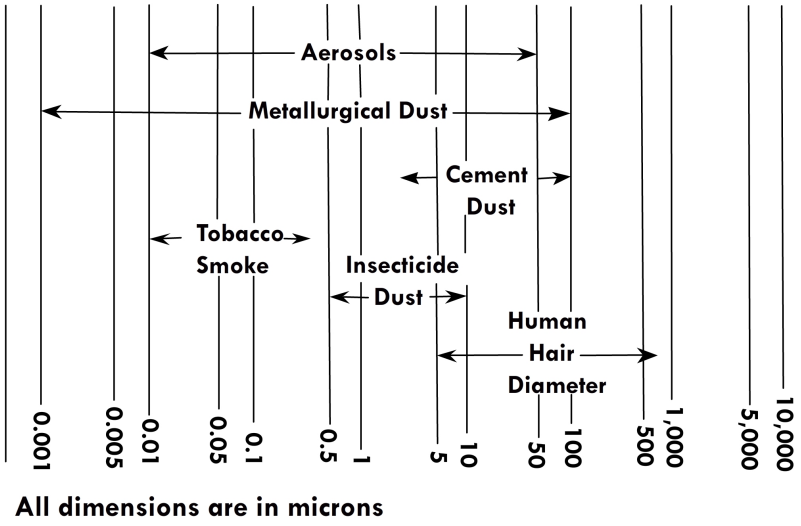


Figure 4: Relative sizes of different airborne contaminants. The units are in microns. Cleanroom classifications are based on the maximum size of particles that are filtered. Smaller clean room numbers are better, since this means that the maximum allowable size is smaller. Adapted from *Microchip fabrication - Peter van Zant.*

5. Static charge
6. Process equipment

3 Clean room design

Air is the most common source of contaminants. To minimize airborne contaminants, a *cleanroom* is used, which is an *area with a controlled level of contaminants*. This is specified by the *number of particles per unit vol, below a specified particle size*. The relative sizes of different airborne contaminants are shown in figure 4. There are different standards and classifications for cleanrooms. One commonly used standard is the US FED STD 209E standard. There is also an ISO standard. These standards mention the number of particles of a given size that are permitted per unit volume, tabulated in 2. The particle sizes for the US FED STD 209E standard are shown in figure 5. The clean room standards are on a log scale. Smaller class number

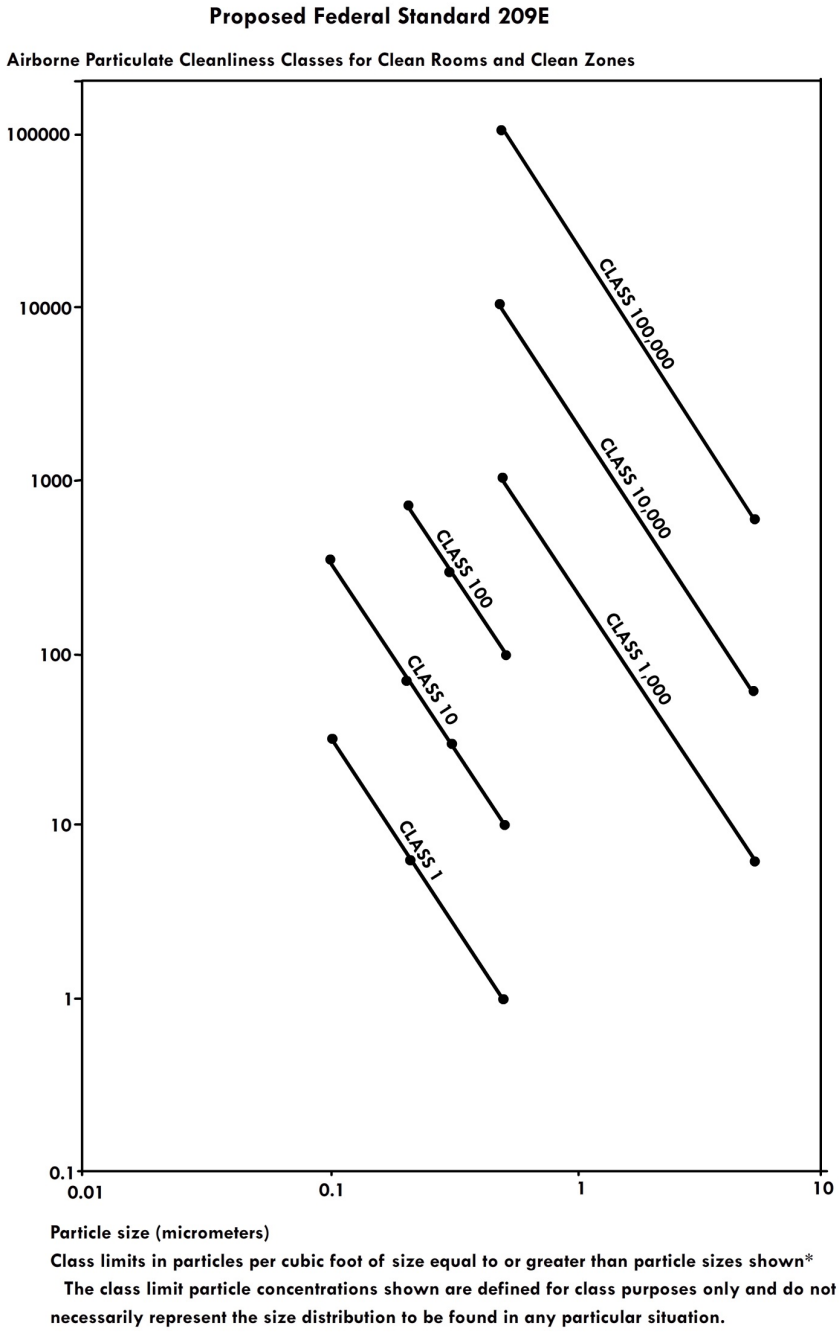


Figure 5: Particles sizes and densities for different FED STD 209E. The y-axis refers to the particle sizes that are permissible, while the x-axis gives the relative concentrations. Adapted from *Microchip fabrication - Peter van Zant.*

Table 2: ISO clean room standards and US FED STD equivalents. The clean room classifications are linked to the size of the particles, see figure 4. Different parts of a fab can have different clean room classifications. Source *http://en.wikipedia.org/wiki/cleanroom*

ISO Class	maximum particles per m^3		**FED STD 209E equivalent**
	$\geq$ 0.1 μm	$\geq$ 1 μm	
ISO 1	10	0.083	
ISO 2	100	0.83	
ISO 3	1000	8.3	Class 1
ISO 4	10000	83	Class 10
ISO 5	10^5	832	Class 100
ISO 6	10^6	320	Class 1000

is better as far as contamination control is concerned. Typically, different parts of the fab have different classifications. In the portion where the wafers are exposed, the highest class is required (i.e. the smallest number).
There are different clean room designs that are available and implementable. The goal of the design is to minimize contamination while having maximum utilization of the available area.

1. Ballroom design
2. Tunnel design
3. Mini-environments
4. Wafer isolation technology (WIT)

The earliest clean room was of the ballroom design. In this design, the fabrication facility is built as one common area (a ballroom)with different workstations or hoods for each process. HEPA (high efficiency particulate attenuation) filters are used in the hoods to minimize contamination. The design is similar to chemical hoods found in most labs, and is shown in figure 6. With increase in integration, the number of processes required for IC fabrication has also increased. This means more processing stations/equipments have to be packed in the fab. Also, with device size shrinkage, clean room requirements became more stringent. So, the ballroom design was replaced by the *tunnel design*.
In the tunnel design, the clean room is divided into a clean area, called the **bay or the tunnel**, and the region separating two bays is called the **chase**. HEPA filters are mounted in the ceiling of the bay areas, as shown in figure

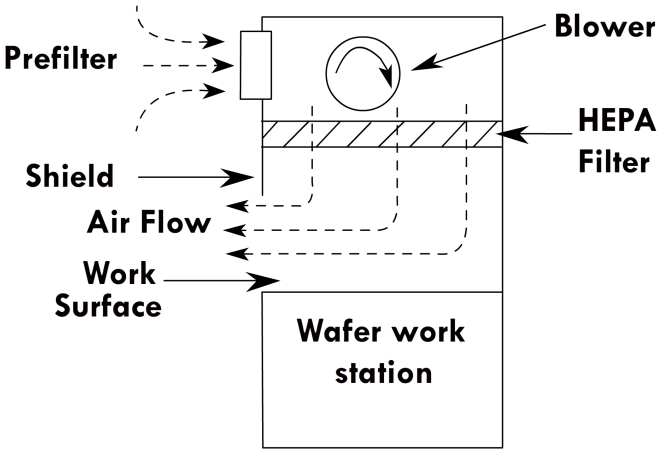


Figure 6: Hood design for wafer work station with vertical laminar flow HEPA filters. Earlier generations of IC fabrication used work stations like these, with the wafers being physically carried from one station to the next. These have since been replaced by automatic wafer carriers. Adapted from *Microchip fabrication - Peter van Zant.*

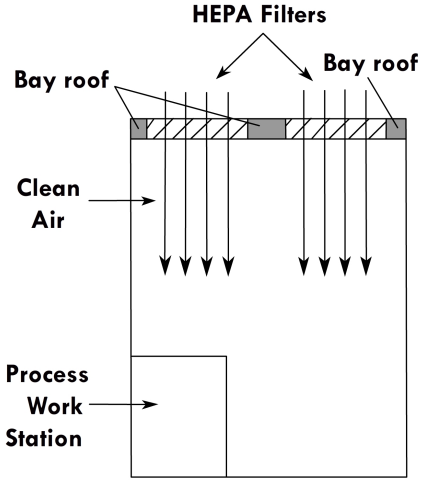


Figure 7: HEPA filters on top of the bay area. The fab is divided into bays (process work stations) and chases (service areas) and clean air flows down the bay area. Adapted from *Microchip fabrication - Peter van Zant.*

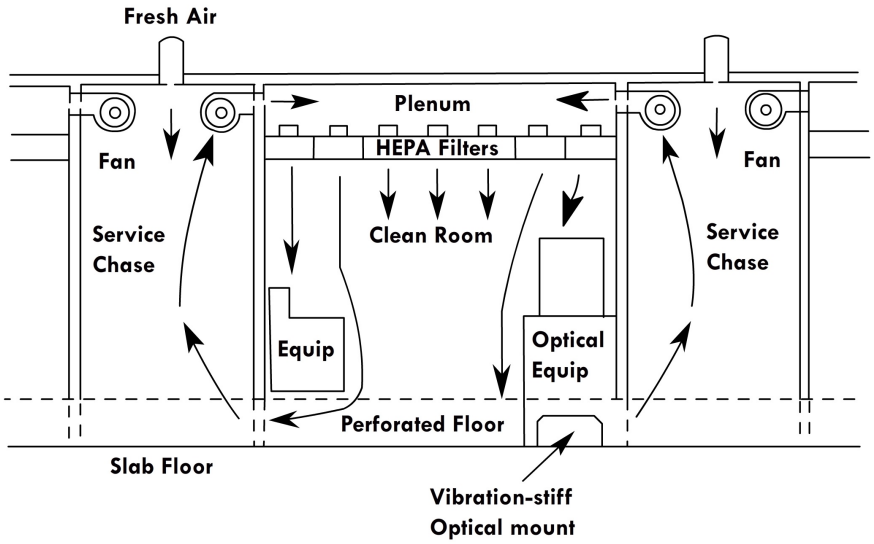


Figure 8: Laminar flow clean room design showing both the bays and chases. The chase refers to the service areas, usually behind the tool, used for maintenance work. In earlier designs, the bays and chases were physically separated by walls, but now the whole fab is built as one large area, back to the *ballroom design*. Adapted from *Microchip fabrication - Peter van Zant.*

7. The chase area is used for maintenance work on the process equipment. The drawback of this design is that it occupies a lot of space, since there must be a physical separation (wall) between the bay and chase.
The current clean rooms go back to the ballroom design. The bay and chase areas are still defined, but they are not physically separated. On the other hand, airflow is regulated in such a way that air flows up from a perforated floor through the chase regions, through HEPA filters and clean air flows down in the bay areas. This is shown in figure 8. The area below the fab is called the *sub-fab*. Power equipment, plumbing, vacuum pumps, process gas and chemical canisters are located in the sub-fab. The sub-fab is located below the perforated floor so that air that flows down in the chase goes to the sub-fab. Blowers are located to blow the air back up through the chase area. There is also a raised metal floor in the fab where wiring is located. This is located above the perforated floor.
In the current clean room design, to ensure minimal contamination to the wafers, they are not exposed within the fab, except in highly regulated areas. Inside the process equipment, wafers are exposed in enclosures called *wafer mini-environments*. These mini-environments are sealed to the fab air (either by vacuum or by excess pressure) so that contamination is minimized.

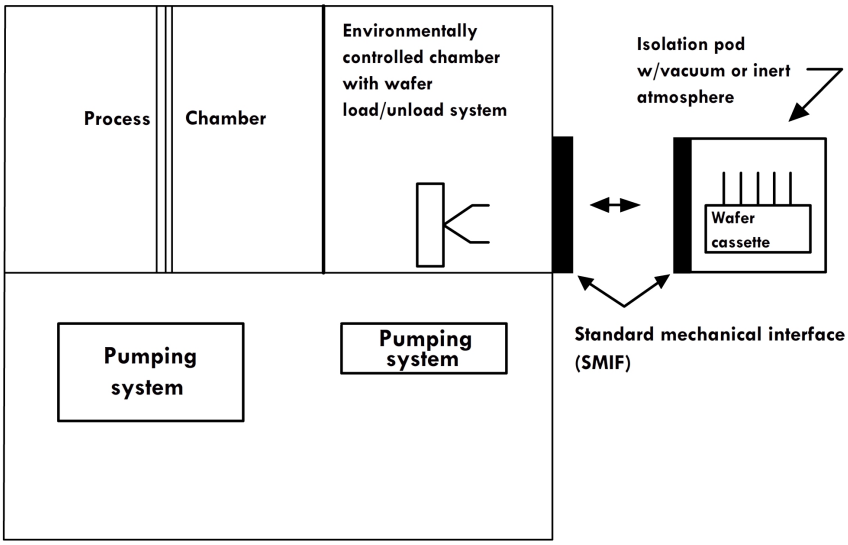


Figure 9: Process tool with mini-environment where wafers are exposed for loading in the tool. Wafers are loaded as cassettes into a environmentally controlled chamber and then individual wafers are loaded in the tool. These areas are usually isolated from the fab by using a pumping system. Adapted from *Microchip fabrication - Peter van Zant.*

The wafer handling process is automated, so that the human operator does not control the movement and loading of the wafers. Figure 9 shows a typical process tool along with the wafer mini-environment. The tool could be a furnace, for growing thermal oxides. Wafers are transferred to the furnace from a previous operation, using FOUPs. In most commercial fabs, the transfer process is automated and takes places using *overhead vehicles* (OHVs). The wafer mini environment is located in front of the furnace and is physically connected to it. The FOUPS are transferred to the mini environment, where the FOUPs are opened and individual wafers transferred for processing. Once processing is done, wafers are transferred back to the FOUPs and then moved on to the next step using the OHVs.

Table 3: Resistivity of water vs. concentration of dissolved ions. Concentrations are in *ppm*. The data values are sourced from *Microchip fabrication - Peter van Zant.*

Resistivity ($\Omega\ cm$)	**Dissolved solids** (ppm)
$1.8\times\ 10^7$	0.028
$1.5\times\ 10^7$	0.033
$1\times\ 10^7$	0.05
$1\times\ 10^6$	0.5
$1\times\ 10^5$	5
10,000	50

4 Clean room materials

4.1 Process water

Water is used extensively in fabrication e.g. in any cleaning process. Typically, wafers are rinsed in water to remove excess chemicals, after a process step, and then dried in nitrogen. This procedure is repeated in many stages during the fabrication process. Normal water contains dissolved minerals, particulates, organics and dissolved gases that make it unsuitable for use in the fab. Dissolved minerals can contain electrically active ions, simple common salt contains Na^+ ions, an MIC, that can destroy the wafer functionality, while particulates and organics can increase contamination. These chemicals have to be removed before use in the fab and the purified water used is called **deionized water** (DI water). The purity of DI water is given by its resistivity. Table 3 lists the resistivity vs. concentration of dissolved ions. Typical DI water used in the fab has a resistivity of 18 $M\Omega\ cm$, so that dissolved ions have a concentration less than 0.03 *ppm* or 30 *ppb*. For comparison, regular tap water has a resistivity of 0.004 $M\Omega\ cm$, so nearly 3 orders of magnitude lowering of impurity concentration is desired. There are a number of filtration steps to achieve this. Figure 10 shows a deionized water purification system.

4.2 Process chemicals and gases

Chemicals like acids, bases, solvents, resists, and strippers are used for different steps in the fabrication process. Common contaminants in these chemicals, like trace metals, particulates, and other chemicals can damage the wafers. There are established standards for chemicals used for IC fabrication, these are called *electronic or semiconductor grade chemicals* and have

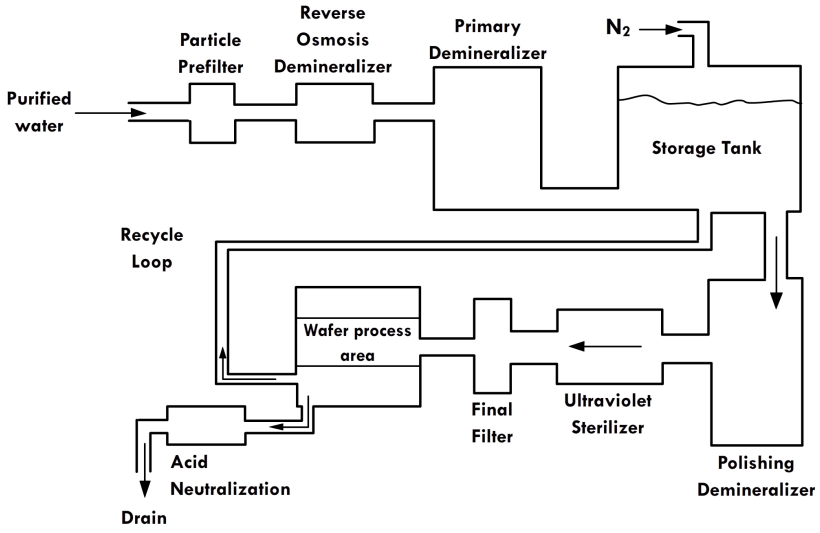


Figure 10: Design of a deionized water system in the fab for removal of impurities. The system can be designed for each individual tool or for a set of tools. The purity level depends on the application. Adapted from *Microchip fabrication - Peter van Zant.*

a higher purity requirement than standard lab chemicals. The primary concern, as in DI water, is the concentration of the MICs. These levels should be in the *ppm* or *ppb* range. Specifications sheet for electronic grade 2-propanol, used as a solvent, is shown in figure 11. Most trace metals have concentration in the *ppb* level. Apart from pure chemicals, their delivery to the fab is also important. Bulk chemical delivery (BCD) systems are setup for this. They are used for providing cleaner chemicals at a lower cost and to ensure quality control.

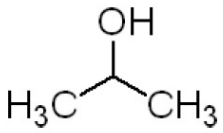
In addition to process chemicals, process gases are also used extensively in the fab. Again, these should be of high purity and this is specified by their *assay number*. *Six 9's purity* (99.999999% pure) gases are the highest purity available and usually two to six 9's pure gases are used. For gases, the piping system is also important. Gas system use stainless steel pipes to minimize outgassing from the metal and also reaction of the metal with the process gas.

Product Specification

Product Name:
2-Propanol – electronic grade, 99.999% trace metals basis

Product Number: **733458**
CAS Number: 67-63-0

Formula: C3H8O
Formula Weight: 60.1 g/mol



TEST	Specification
Appearance (Color)	Colorless
Appearance (Form)	Liquid
Infrared spectrum	Conforms to Structure
Purity (GC)	≥ 99.9 %
Acetone	≤ 0.01 %
Water (by Karl Fischer)	≤ 0.05 %
Residue on Evaporation	≤ 0.0005 %
Free Acid as Acetic Acid	≤ 0.001 %
Aluminum (Al)	≤ 10 ppb
Antimony (Sb)	≤ 10 ppb
Arsenic (As)	≤ 10 ppb
Barium (Ba)	≤ 10 ppb
Beryllium (Be)	≤ 10 ppb
Bismuth (Bi)	≤ 10 ppb
Boron (B)	≤ 10 ppb
Cadmium (Cd)	≤ 10 ppb
Calcium (Ca)	≤ 10 ppb
Chromium (Cr)	≤ 10 ppb
Cobalt (Co)	≤ 10 ppb
Copper (Cu)	≤ 10 ppb
Gallium (Ga)	≤ 10 ppb
Germanium (Ge)	≤ 10 ppb
Gold (Au)	≤ 10 ppb

Figure 11: Product specification for Electronic grade 2-propanol sourced from *Sigma-Aldrich, product no. 733458*. Concentration of metallic impurities are in ppb.

5 Wafer-surface cleaning

Clean wafers are needed at every step of the fabrication process. Wafers after processing at one step, have to be cleaned (and if needed inspected) before moving to the next process step. There are four main type of contaminants that can be added during processing

1. Particulates
2. Organic residues
3. Inorganic residues
4. Unwanted organic layers

The wafer cleaning process must do the following

1. Remove all surface contaminants (listed above)
2. Not etch or damage the wafer surface, in any way
3. Be, safe, economical, and ecologically acceptable
4. Must not be time-consuming

In the front end of the line (FEOL), the cleaning should not affect surface roughness (variation should be less than 1 nm) and should also maintain electrical characteristics. In the back end of the line (BEOL), electrical shorting is the main concern during cleaning. Typical FEOL cleaning steps are shown below

1. Particle removal (mechanical)
2. Chemical clean (H_2SO_4, H_2O_2)
3. Oxide removal (dilute HF)
4. Organic and metal removal
5. Alkali metal and hydroxide removal
6. Rinse steps, typically DI water
7. Drying - N_2 gas, room temperature or hot

Table 4: Standard RCA clean recipes. These are used to remove the native oxide layer on Si and leave a hydrogen terminated surface. Recipe was adapted from *Microchip fabrication - Peter van Zant.*

RCA clean type	**Parts by volume**
Standard clean (SC-1)	5: DI water 1: 30% Hydrogen peroxide 1: 30% Ammonium hydroxide
Process 70 °C for 5 min	
Standard clean 2 (SC-2)	6: DI water 1: 30% Hydrogen peroxide 1: 37% Hydrochloric acid
Process 70 °C, 5-10 min	

A common chemical cleaning procedure, used for removing organic and inorganic residue from silicon wafers, is the *RCA clean*. This was developed in the 1960s, by Werner Kern, an engineer at Radio Corporation of America (RCA). The steps involved in RCA clean are tabulated in 4. There are a large number of variations available to this process. When an oxide free surface is needed, HF is used after the RCA clean process to remove the native oxide and provide hydrogen passivation.