Universal Serial Bus 3.2
Electrical Compliance Test Specification

Date: June 30, 2026

Revision: 1.8

Revision History:

Revision	Issue Date	Comments
1.0	01.01.2023	Release to USB-IF ECWG by Lev Kolomiets
1.1	31.05.2023	Added clarification on some of the tests by Stav Gutman
1.2	26.08.2024	Scope capture examples have been added, Retimer and general flow processes have been elaborated, and various other enhancements have been implemented by Stav Gutman
1.3	9.10.2024	Updated link training to BLR compliance in Retimers (Gen1 or Gen2 sequence).
1.4	22.11.2024	Added non-BLR Retimer (SRIS) Gen1 TX compliance testing support, reference to technical sessions slides.
1.5	07.01.2025	Fixed the number of high-speed patterns of the optional Gen2 link training option for TX BLR to align with the Gen1 link requirement.
1.6	01.04.2025	Added links to legacy connector topologies, and missing s-parameters files reference. Updated link to USB-IF USB3.2 TX embedding files. Removed the Micro-AB embedding reference from the TX Eye tests 'Reference Equalizer' Gen1/2 tables.
1.7	24.09.2025	Updated the correct USB3.2 fixtures USBIF reference. Updated the correct link to the Gen2 legacy connector topologies. Removed the Micro-AB embedding reference from the RX Eye tests 'Reference Equalizer' Gen1/2 tables.
1.8	30.06.2026	Updated the RX JTOL test names to x1 (Gen1x1 and Gen2x1 JTOL). Changed the TX x2 lane-to-lane skew test classification to Informative.

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Acronyms

Acronym	Definition
BLR	Bit-Level Retimer
SRIS	Separate Reference Clock Independent SSC
BER	Bit Error Rate
BERT	Bit Error Rate Tester
BW	Band Width
CDR	Clock Data Recovery
DUT	Device Under Testing
SSC	Spread Spectrum Clock
TJ	Total Jitter
UI	Unit Interval
DJ	Deterministic Jitter
RJ	Random Jitter
PPM	Parts Per Million
IL	Insertion Loss

1 Introduction

This document contains the specification of procedures, tools, and criteria for testing compliance of Hosts, Hubs, Devices and Retimers according to the Universal Serial Bus 3.2 Base Spec Version 1.0. These criteria address the electrical requirements for a USB3.2 physical layer design. Test descriptions provide a high-level overview of the tests that are performed to check the compliance criteria. The descriptions are provided with enough detail so that a reader can understand what the test does. The descriptions do not describe the actual step-by-step procedure to perform the test.

1.1 Related Documents

[1] Universal Serial Bus 3.2 Specification, revision 1.1, June 2022
[2] Universal Serial Bus Type-C Cable and Connector Specification, revision 2.3, October 2023
[3] Universal Serial Bus Specification, Revision 2.0, April 27, 2000.
[4] USB-IF USB 2.0 Electrical Test Specification, Version 1.07, February 2019
[5] USB3p2_Retimer_CTS_Draft_Rev1
[6] USB3p2_Retimer_Q_&_A
[7] USBIF_USB3p2_new_CTS_General_intro
[8] USBIF_USB3p2_new_CTS_Retimer_TX_intro
[9] USBIF_USB3p2_new_CTS_Retimer_RX_intro
[10] USB3p2_SigTest_User_Manual

1.2 USB 2.0 Compliance

USB 2.0 testing is required for USB 3.2 DUTs and is covered by a separate compliance testing program. Refer to [3] and [4] for details.

1.3 Engineering Change Notice (ECN)

It is the responsibility of the implementer to ensure alignment with the available Engineering Change Notices (ECNs). The relevant ECNs can be accessed at the following path.
https://www.usb.org/document-library/usb-32-revision-11-june-2022

2 Test Equipment

2.1 Overview

All equipment used for testing shall comply with the requirement lists specified below.

This includes the primary equipment that is used in the USB3.2 authorized test centers and should also, if possible, be used by the end user for self-testing.

Other configurations and equipment may be used for self-testing if that equipment and the processes meet all the stated and implied requirements and permit an equivalent level of testing.

2.2 Test Equipment Requirements

All test equipment requires calibration to ensure accurate and repeatable results. Equipment shall be calibrated prior to, and if necessary, during the test procedure.

2.2.1 Test Point Access Boards

To gain access to the required signals, a variety of test point access boards are required. Test Point Access boards provide test points for the pins on the USB3.2 connector and an easy way to control the DUT.

Refer to https://www.usb.org/compliancetools for fixture kits details.

2.2.2 Real Time Scopes

Minimum Required Test Equipment Capabilities:

- DC to 16GHz, -3db bandwidth or greater
- 80G sample/sec Sampling rate or greater, sampling 2 channels simultaneously
- Sample memory: 50M samples per channel or greater
- Embedding/de-embedding capability

Recommended Test equipment Capabilities

- 1st and 2nd order CDR capability
- Equalization and DFE
- Jitter measurement

2.2.3 Signal Generator

Minimum Required Test Equipment Capabilities:

- Generate USB3.2 LFPS as defined in section 6.9 and Table 7.5.4.5.1 of USB3.2 Rev 1.0 Specification
- Memory > 16 Mbit

Recommended Test equipment Capabilities

- Dual channel differential signal generation
- Store 5 user defined LFPS patterns in non-volatile memory

2.2.4 BERT (Bit Error Tester)

Generate USB3.2 signal with a variety of patterns, jitter injection capability and Analyze Looped back data.

Minimum Required Test Equipment Capabilities:

- Data rates ≥ 10Gbps
- Data patterns: All USB3.2 Specification defined pattern types, full complete link training and management capability, PRBS15, PRBS31, Square wave
- Differential swing range: 0 – 2Vp-p in 10mV steps
- Rise Time ≥ 10 ps (20%-80%)
- Intrinsic jitter ≤ 400 fS RMS
- Equalization
- SSC spread deviation from 0.03% down to -0.53%
- Injection of Rj and SJ (single/dual tone) sources
- Identify single Bit Error in looped back data pattern

2.2.5 DC Block

Required Test Equipment Capabilities:

- Capacitance of 135nF–265nF (220nF is recommended)
- Bandwidth of at least 16GHz
- Insertion Loss @ 16GHz < 1 dB
- Cutoff frequency (3dB) = $\frac{1}{2*\pi*R*C} = \frac{1}{2*\pi*50*220e-9} = 14.468\ kHz$

Recommended Test equipment Capabilities

- Independent Dual Channel Generator and Error detector control including full dual lane link training capability
- Channel to channel flow control
- Arbitrary SSC profile

3 Transmitter Testing

- Transmitter compliance testing is defined at the output of a compliance test fixture at the TP2 reference point and at the TP3 reference point for captive cable DUT.
- Long Compliance Channel embedding is performed by the test equipment or Sigtest using the USB-IF provided s-parameters files or official fixture kit physical channel for non-Type-C connectors.

The following sections provide detailed information on the setup and testing of the USB3.2 parameters. In the event of a discrepancy, the USB3.2 Specification prevails.

Table 1 Tx USB3.2 Electrical Compliance Test Points Definition

Test Point (TP)	Description
TP1	Transmitter silicon pad
TP2	Transmitter port connector mid-point
TP3	Receiver port connector mid-point
TP4	Receiver silicon pad
TP1Ro, TP3Ro	Re-timer transmitter silicon pad
TP1Ri, TP3Ri	Re-timer receiver silicon pad

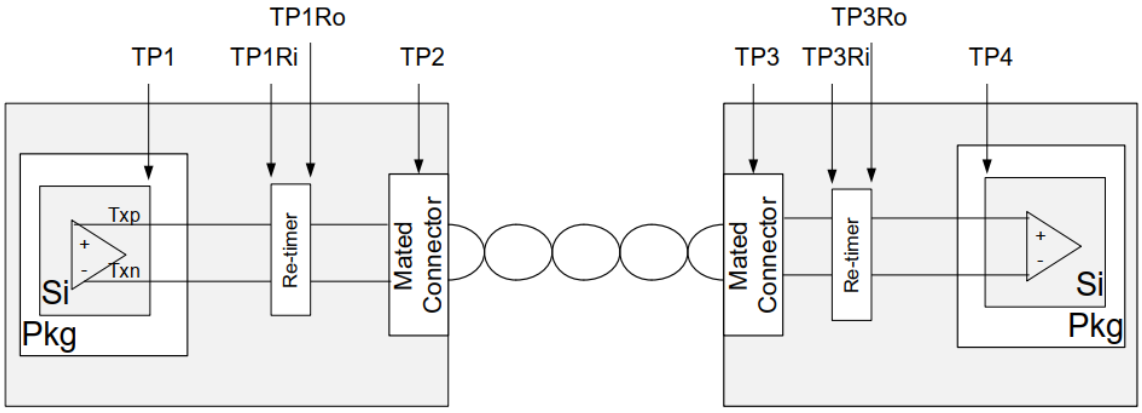


Figure 1 Tx USB3.2 Electrical Compliance Test Points Definition

3.1 Gen1 Low Frequency Periodic Signaling (LFPS) TX Test

This test verifies that the low frequency periodic signal (LFPS) transmitter meets the timing and voltage requirements when measured at the compliance test port.

Overview of Test Steps

1. Connect the DUT to a simple breakout test fixture.
2. Disconnect bus power if the DUT is a bus powered device.
3. In the case of Gen1 DUT, power on the device under test (connect bus powered if DUT is a bus powered device) and let it pass through the Rx.Detect state to the Polling.LFPS substate.

   In the case of a Gen2 DUT perform this step while transmitting Polling.LFPS to the configuration lane RX of the DUT.
4. In case of a Gen2 DUT, trigger on the Polling.LFPS that comes after the SCD1 pattern, in case of a Gen1 DUT trigger on the initial Polling.LFPS bursts sent by the DUT.

   In both cases, capture the first five Polling.LFPS bursts for analysis.
5. Measure the following LFPS parameters and compare against the USB 3.2 specification requirements: tBurst, tRepeat, tPeriod, tRiseFall2080, Duty cycle, $V_{CM-AC-LFPS}$, and $V_{TX-DIFF-PP-LFPS}$. For these measurements the start of an LFPS burst is defined as starting when the absolute value of the differential voltage has exceeded 100 mV and the end of an LFPS burst is defined as when the absolute value of the differential voltage has been below 100 mV for 50 ns. tPeriod, tRiseFall2080, Duty cycle, $V_{CM-AC-LFPS}$, and $V_{TX-DIFF-PP-LFPS}$ are only measured during the period from 100 nanoseconds after the burst start to 100 nanoseconds before the burst stop, refer to appendix 3 for implementation.

In case of **captive cable devices,** it is considered that the captive cable shall comply with USB Type-C Specification (R2.3 October 2023) section 3.7.2.1.1, LFPS maximum frequency is 50MHz thus the expected IL is -1[dB].

- Low Power transmitter captive cable device at TP2 is not accessible thus effective TP3 shall comply with the following limit: 0.352[V] (instead of the 0.4[V] VTX-DIFF-PP-LFPS-LP lower limit).

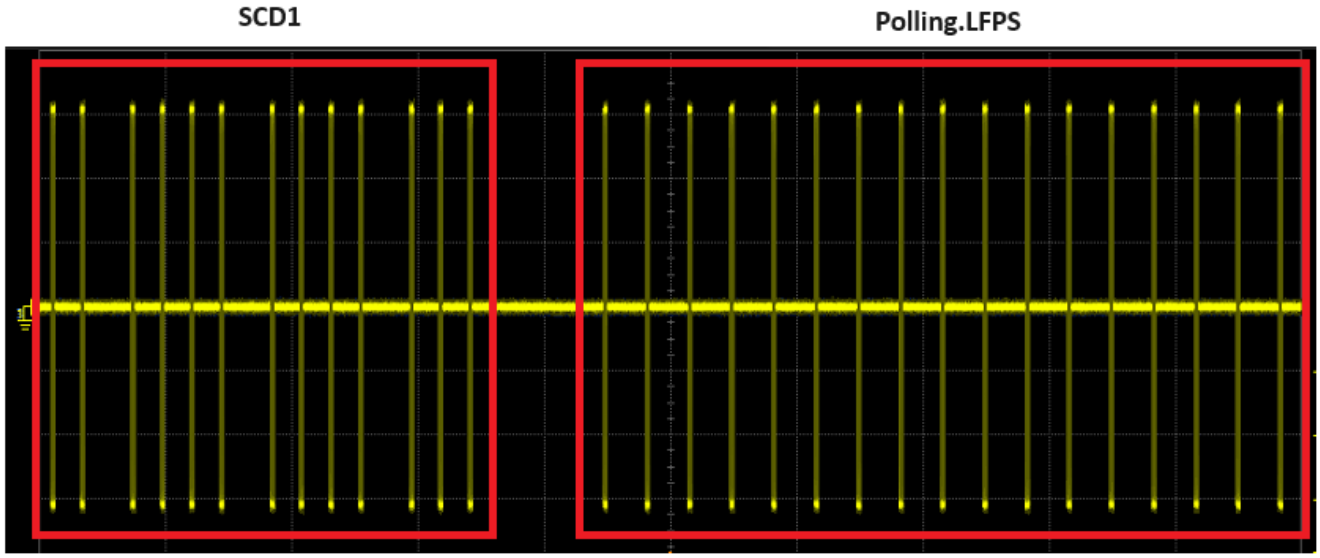
6. For **captive cable devices** Repeat steps **1 to 5** and compare tBurst, tRepeat, tPeriod, tRiseFall2080, Duty cycle, VCM-AC-LFPS. VTX-DIFF-PP-LFPS is compared against specified limits in the spec reference tables mentioned below. A **Captive device** will pass if in compliance to this step.
7. If the DUT is Type-C repeat all testing with the alternate Tx path by changing the CC state or by flipping the fixture.

Spec References

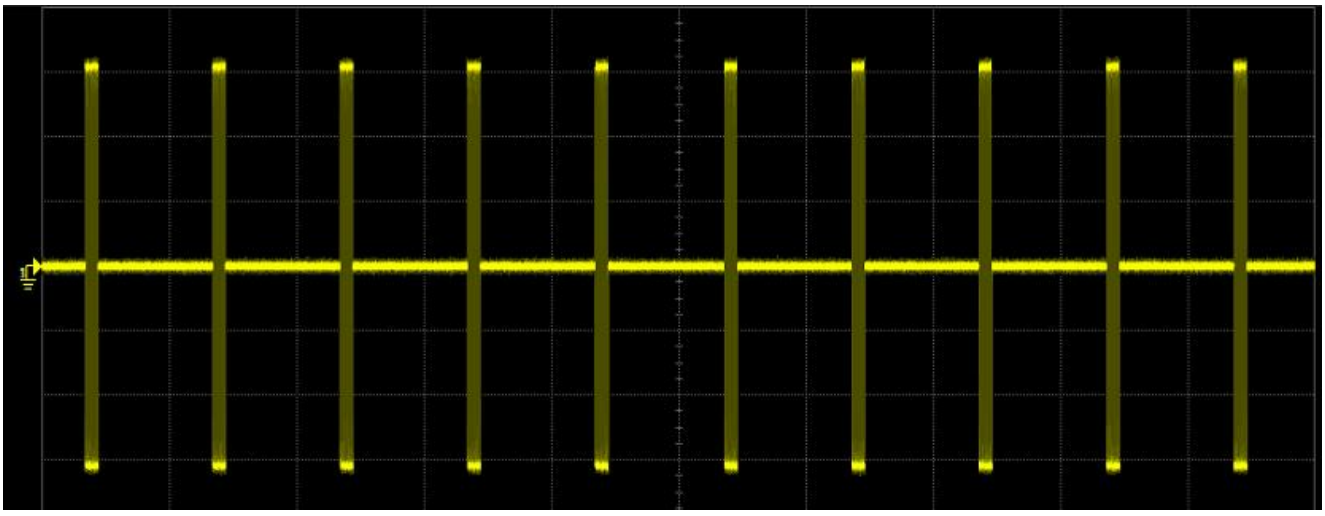
- USB 3.2 Specification, revision 1.1
  - Table 6-29
  - Table 6-30

Note: In case of an embedded Retimer DUT system, refer to Appendix 4.

- Scope capture example of the "Polling.LFPS" to be analyzed in the case of a Gen2 DUT



- Scope capture example of the "Polling.LFPS" to be analyzed in the case of a Gen1 DUT



3.2 Gen2 Low Frequency Periodic Signaling (LFPS) TX Test (Gen2 DUT only)

This test verifies that the low frequency periodic signal (LFPS) transmitter meets the timing and voltage requirements when measured at the compliance test port.

Overview of Test Steps

1. Connect the DUT to a simple breakout test fixture.
2. Disconnect bus power if the DUT is a bus powered device.
3. Power on the device under test (connect bus powered if DUT is a bus powered device) and let it pass through the Rx.Detect state to the Polling.LFPS substate.
4. Trigger on initial SCD1 pattern and capture the first two SCD1 patterns for analysis.
5. Measure the following LFPS parameters and compare against the USB 3.2 specification requirements: tBurst, tRepeat, tPeriod, tRiseFall2080, Duty cycle, $V_{CM\text{-}AC\text{-}LFPS}$, and $V_{TX\text{-}DIFF\text{-}PP\text{-}LFPS}$. For these measurements the start of an LFPS burst is defined as starting when the absolute value of the differential voltage has exceeded 100 mV and the end of an LFPS burst is defined as when the absolute value of the differential voltage has been below 100 mV for 50 ns. tPeriod, tRiseFall2080, Duty cycle, $V_{CM\text{-}AC\text{-}LFPS}$, and $V_{TX\text{-}DIFF\text{-}PP\text{-}LFPS}$ are only measured during the period from 100 nanoseconds after the burst start to 100 nanoseconds before the burst stop.
6. Disconnect test fixture and bus power if the DUT is a bus powered device.
7. Connect DUT Rx lanes of the simple breakout fixture to signal generator transmitting repeating sequence of:
   a. 2-32 x SCD1
   b. 2-32 x SCD2
   c. 4-32 x LBPM with PHY Capability
   d. 4-32 x LBPM with PHY Ready

   Voltage and Timing parameters of the signal generator should be set to typical USB3.2 specification values
8. Trigger on the initial SCD2 pattern and capture two SCD2 patterns for analysis
9. Repeat measurement as described in **step 5**
10. Repeat setup steps **6 and 7**
11. Trigger on the initial LBPM PHY capability pattern and capture first two LBPM PHY capability patterns and first two LBPM PHY ready patterns for analysis
12. Measure the following LBPM parameters and compare against the USB 3.2 specification requirements: tLFPS-0, tLFPS-1, tPWM, tRiseFall2080, Duty cycle, $V_{CM\text{-}AC\text{-}LFPS}$, and $V_{TX\text{-}DIFF\text{-}PP\text{-}LFPS}$. For these measurements the start of an tLFPS-0 or tLFPS-1 burst is defined as starting when the absolute value of the differential voltage has exceeded 100 mV and the end of an tLFPS-0 or tLFPS-1 burst is defined as when the absolute value of the differential voltage has been below 100 mV for 50 ns. tLFPS-0, tLFPS-1, tPWM, tRiseFall2080, Duty cycle, $V_{CM\text{-}AC\text{-}LFPS}$, and $V_{TX\text{-}DIFF\text{-}PP\text{-}LFPS}$ are only measured during the

period from 100 nanoseconds after the tLFPS-0 or tLFPS-1 burst start to 100 nanoseconds before the burst stop, refer to appendix 3 for implementation.

In case of **captive cable devices,** it is considered that the captive cable shall comply with USB Type-C Specification section (R2.3 October 2023) 3.7.2.1.1, LFPS maximum frequency is 50MHz thus the expected IL is -1[dB].

- Low Power transmitter captive cable device at TP2 is not accessible thus effective TP3 shall comply with the following limit: 0.352[V] (instead of the 0.4[V] VTX-DIFF-PP-LFPS-LP lower limit).

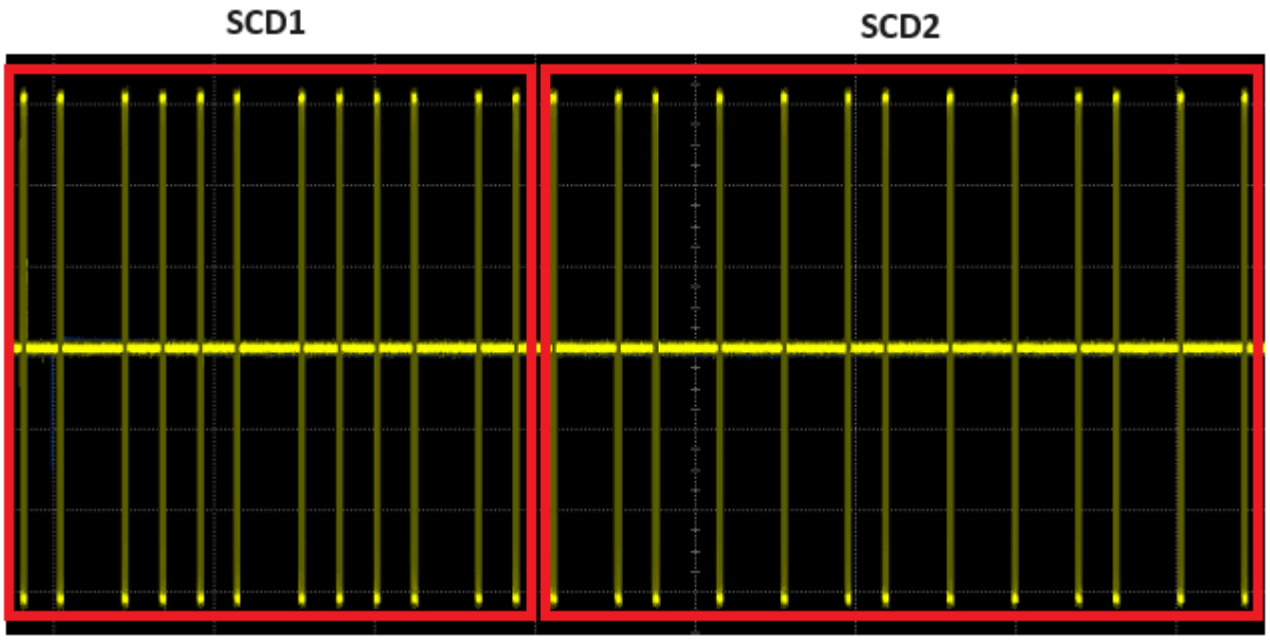
13. For **captive cable devices** Repeat steps **1 to 12** and compare tBurst, tRepeat, tPeriod, tLFPS-0, tLFPS-1, tPWM, tRiseFall2080, Duty cycle, VCM-AC-LFPS. VTX-DIFF-PP-LFPS is compared against specified limit in the spec reference tables mentioned below. A **Captive device** will pass if in compliance to this step.
14. If the DUT is Type-C repeat all testing with the alternate Tx path by changing the CC state or by flipping the fixture.

Spec References

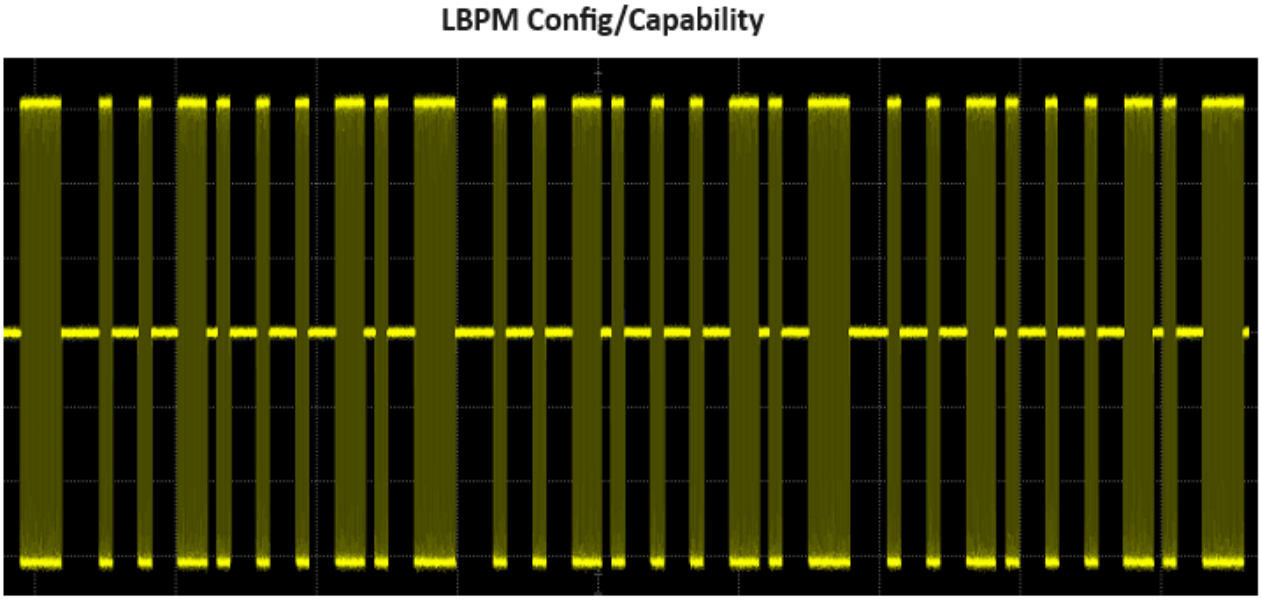
- USB 3.2 Specification, revision 1.1
    - Table 6-29
    - Table 6-32
    - Table 6-33

Note: In case of an embedded Retimer DUT system, refer to Appendix 5.

- Scope capture example of the "SCD1/SCD2" to be analyzed

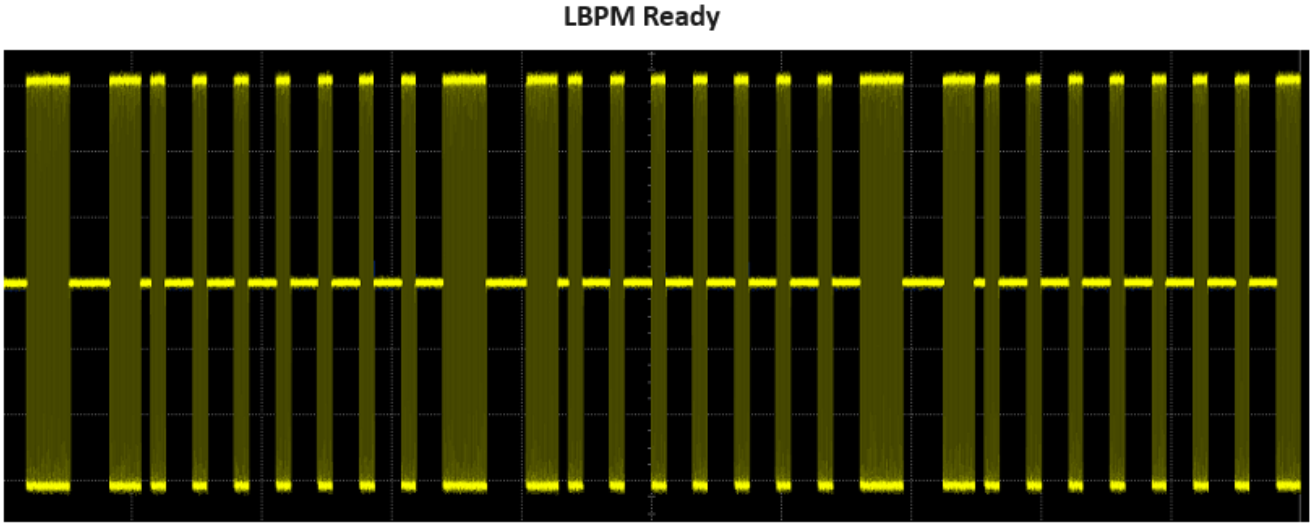


- Scope capture example of the "LBPM Config/Capability" to be analyzed



Note: LBPM Config/Capability first two bits [b1:b0] values are [0,0] accordingly. (Table 7-13, USB 3.2 Specification, revision 1.1)

- Scope capture example of the "LBPM Ready" to be analyzed



Note: LBPM Ready first two bits [b1:b0] values are [0,1] accordingly. (Table 7-13, USB 3.2 Specification, revision 1.1)

3.3 Gen1 Data Eye and Jitter

This test verifies that the transmitter meets the eye width, deterministic jitter and random jitter requirements when measured at the compliance test port with nominal transmitter equalization and after processing with the appropriate channels and post processing as shown in Table 2.

Connector Type	Channel	Reference Equalizer
Std-A	Device Under Test >> USB3.2 Host Fixture 1A >> SCOPE (Embed Cable + Device PCB) USB3_HOST_TEST_SPARAMS.s4p	Long Channel
Std-B	Device Under Test >> USB3.2 Device Fixture 1A >> SCOPE (Embed 7dB Cable + Host PCB) USB3_DEVICE_TEST_SPARAMS.s4p	Long Channel
Type-C (Host)	Device Under Test >> USB3.2 Host Fixture 1C >> SCOPE (Embed 7dB Cable + Device PCB) SSGen1_TxComp12p7dB_Embedding.s4p	Long Channel
Type-C (Device)	Device Under Test >> USB3.2 Device Fixture 1C >> SCOPE (Embed 7dB Cable + Host PCB) SSGen1_TxComp12p7dB_Embedding.s4p	Long Channel
Micro-B	Device Under Test >> USB3.2 Device Fixture 1A >> SCOPE (Embed 7dB Cable + Host PCB) SSGen1_TxComp11p5dB_Embedding.s4p	Long Channel
Tethered/Captive (Standard A Plug)	Device Under Test >> USB3.2 Captive Cable Device Fixture Type-A >> SCOPE (Embed Host PCB) SSGen1_TxComp8p5dB_Embedding.s4p	Long Channel
Captive (Standard C Plug)	Device Under Test >> USB3.2 Captive Device Fixture 1C >> SCOPE (Embed Host PCB) SSGen1_TxComp4p5dB_Embedding.s4p	Long Channel
All Types (except Captive C)	No Channel (USB3.2 Break-out fixture only)	Short Channel
Captive (Standard C Plug)	No Channel (USB 3.2 Captive Device Fixture Type-C)	Short Channel

Table 2 - Tx Gen1 Channels and Reference Equalizer for Testing Device Types

Note: For connection topologies refer to https://www.usb.org/sites/default/files/documents/usb3p1_fixture_topologies_11-8-2017_0.pdf, https://www.usb.org/sites/default/files/documents/superspeedtesttopologies.pdf, https://fixturesolution.com/wp-content/uploads/2024/04/FS-USB3.2-Gen1-Test-Topologies.pdf
Note: Refer to https://www.usb.org/document-library/usb-32-embedding-files
For S-parameter files used for embedding the long channels when using breakout fixtures. To comprehend noise effects, such as crosstalk, it is up to the DUT manufacturer to make sure that any other links are active for the various DUT types.

Note: Refer to Appendix 1 for the reference equalizer methodology.

Overview of Test Steps

The test runs in the Polling.Compliance substate in the case of SoC.
For Retimers, if the Retimer implements the BLR architecture then the BLR compliance mode shall be used, otherwise, the legacy Polling.Compliance (SRIS) mode shall be tested instead. Perform the following steps.

1. Connect the DUT to a simple break-out test fixture without VBUS supplied.
2. If the DUT is a host or a hub (for testing downstream ports) then run xHSETT and put the host/downstream hub port into compliance mode, in the case of a non-BLR Retimer DUT, the legacy compliance mode shall be used.
3. If DUT has a BLR Retimer (embedded or component with golden host)
    a. Connect BERT output to simple break-out test fixture Rx

    Note: If the BERT is protocol aware it is allowed to just follow the protocol rules in the base specification (interactive link training)

    b. BERT sends either of the following sequences:
        i. Gen2 link flow
            1. 2-32 SCD1
            2. 2-32 SCD2
            3. 4-32 LBPM (w PHY capability set to Gen1x1).
            4. 4-32 LBPM (w PHY ready)
            5. Except typical SSC configuration all other jitter sources are disabled during all transmissions to the device under test. If the device does not go into BLR Compliance, it fails the test.
            6. Transmit 65,536 TSEQ It is preferred for the BERT to transmit as close to 65,536 TSEQ as possible. If a device requires several TSEQ outside this range to pass the test this is a failure.
            7. Transmit 256 – 65,536 TS1. (SYNC, 31 TS1, SKP – repeat to up to 65,536 total TS1)
            8. Transmit 256 – 65,536 TS2 with Loopback (bit 2) and Bit-level re-timer Tx compliance (bit 5) bits asserted in the link configuration field (Table 6-6 in the USB3.2 specification).
        ii. Gen1 link flow
            1. 400 Polling.LFPS (4ms)
            2. 65,536 TSEQ
            3. 256-65,536 TS1
            4. 256-65,536 TS2 with Loopback (bit 2) and Bit-level re-timer Tx compliance (bit 5) bits asserted in the link configuration field

4. Power on the device under test and apply VBUS if the DUT is not a host, let it pass through the Rx.Detect state to the Polling.Compliance or BLR Compliance state.
5. For a non-BLR Retimer port, if the DUT is x2 capable, both lanes must transmit same compliance patterns and promote in sync. When PING.LFPS is applied to configuration lane Rx
6. Transmit the CP0 compliance pattern on the port under test and capture the transmitted waveform on a high-speed oscilloscope over a minimum of 1,000,000 unit intervals (200 μsec) at a sample rate of no more than 25 ps in a single scope capture.
7. Promote compliance patterns by:
    a. DUT w/ BLR Retimer port under test - send 4 x SKP OS (Table 6-12 in the USB3.2 specification) to the RX port of the device under test to cause the compliance pattern to transition to CP1.
    b. DUT w/o BLR Retimer port under test - send a PING.LFPS to the RX port of the device under test (for x2 capable apply to configuration lane only) to cause the compliance pattern to transition to CP1. A single PING.LFPS burst is sent with the following parameters:
        i. 100 nanosecond duration.
        ii. 20 MHz frequency (2 periods).
8. Transmit the CP1 compliance pattern on the port under test and capture the transmitted waveform on a high-speed oscilloscope over a minimum of 1,000,000 unit intervals (200 μsec) at a sample rate of no more than 25 ps in a single scope capture.

The required compliance channel shown in Table 2 for the connector type under test is embedded to the measured CP0 and CP1 data.

The following analysis in steps 9-10 is done applying the appropriate equalizer (shown in Table 2 and elaborated at appendix 1), and JTF (elaborated at appendix 2) in the waveform analysis.

9. Compute the data eye using CP0 and compare it against the normative transmitter specifications contained in the USB 3.2 specification.
10. Compute the total jitter at 10^{-12} BER using the CP0 data to compute a measured Tj and the Rj value from CP1 with the dual-dirac method and compare it against the normative transmitter specification contained in the USB 3.2 specification.

Note: Extrapolate Tj E-12 based on Tj measured with CP0 and CP1 Rj only.

11. Repeat the analysis in steps 9-10 for the short channel and reference equalizer shown in Table 2.

If the DUT is Type-C and is x1 capable repeat all testing with the alternate Tx path by changing the CC state or by flipping the fixture. If Type-C is x2 capable, repeat all testing with other lane Tx without changing CC state.

Spec References

- USB 3.2 Specification, revision 1.1
    - Table 6-20, Figure 6-20
    - Figure 6-1

3.4 Gen1 Spread Spectrum Clocking (SSC)

This test verifies that the transmitter meets SSC profile requirements when measured at the compliance test port with spec required TX equalization. To comprehend noise effects, such as crosstalk, it is up to the DUT manufacturer to make sure that any other links are active for the various DUT types.
Note: A PCI Express host adaptor is tested in a system that provides a 100 MHz PCI Express reference clock with a valid SSC profile and in a system with a 100 MHz PCI Express reference clock that does not have SSC. The host adaptor must pass all tests in both cases. No transmitter testing is done with multiple downstream ports active on hosts/hubs.

Overview of Test Steps

The test runs in the Polling.Compliance substate in the case of SoC.
For Retimers, if the Retimer implements the BLR architecture then the BLR compliance mode shall be used, otherwise, the legacy Polling.Compliance (SRIS) mode shall be tested instead.
Perform the following steps.

1. Connect the DUT to a simple break-out test fixture without VBUS supplied.
2. If the DUT is a host or a hub (for testing downstream ports) then run xHSETT and put the host/downstream hub port into compliance mode, in the case of a non-BLR Retimer DUT, the legacy compliance mode shall be used.
3. If DUT has a BLR Retimer (embedded or component with golden host)
    a. Connect BERT output to simple break-out test fixture Rx

    Note: If the BERT is protocol aware it is allowed to just follow the protocol rules in the base specification (interactive link training)

    b. BERT sends either of the following sequences:
        i. Gen2 link flow
            1. 2-32 SCD1
            2. 2-32 SCD2
            3. 4-32 LBPM (w PHY capability set to Gen1x1).
            4. 4-32 LBPM (w PHY ready)
            5. Except typical SSC configuration all other jitter sources are disabled during all transmissions to the device under test. If the device does not go into BLR Compliance, it fails the test.
            6. Transmit 65,536 TSEQ It is preferred for the BERT to transmit as close to 65,536 TSEQ as possible. If a device requires several TSEQ outside this range to pass the test this is a failure.
            7. Transmit 256 – 65,536 TS1. (SYNC, 31 TS1, SKP – repeat to up to 65,536 total TS1)
            8. Transmit 256 – 65,536 TS2 with Loopback (bit 2) and Bit-level re-timer Tx compliance (bit 5) bits asserted in the link configuration field (Table 6-6 in the USB3.2 specification).

ii. Gen1 link flow

1. 400 Polling.LFPS (4ms)
2. 65,536 TSEQ
3. 256-65,536 TS1
4. 256-65,536 TS2 with Loopback (bit 2) and Bit-level re-timer Tx compliance (bit 5) bits asserted in the link configuration field

4. Power on the device under test and apply VBUS if the DUT is not a host, let it pass through the Rx.Detect state to the Polling.Compliance or BLR Compliance state.
5. For a non-BLR Retimer port, if the DUT is x2 capable, both lanes must transmit same compliance patterns and promote in sync. When PING.LFPS is applied to configuration lane Rx
6. Transmit the CP0 compliance pattern on the port under test.
7. Promote compliance patterns by:
    a. DUT w/ BLR Retimer port under test - send 4 x SKP OS (Table 6-12 in the USB3.2 specification) from to the RX port of the device under test to cause the compliance pattern to transition to CP1.
    b. DUT w/o BLR Retimer port under test - send a PING.LFPS to the RX port of the device under test (for x2 capable apply to configuration lane only) to cause the compliance pattern to transition to CP1. A single PING.LFPS burst is sent with the following parameters:
        i. 100 nanosecond duration.
        ii. 20 MHz frequency (2 periods).
8. Transmit the CP1 compliance pattern on the port under test and capture the transmitted waveform on a high-speed oscilloscope over a minimum of 1,000,000 unit intervals (200 μsec) at a sample rate of no more than 25 ps in a single scope capture.
9. Compute the phase jitter for the captured waveform and apply a 60*33KHz 3dB cutoff frequency, 40 dB/decade Low Pass Filter to the phase jitter.
10. Use the filtered phase jitter to check that the SSC fundamental frequency is between 30 and 33 KHz.
11. Take the derivative of the filtered phase jitter and convert to ppm.
12. Check that twice maximum difference between points that are 0.5 μs apart in the derivative of the filtered phase jitter is less than 1250 ppm.
13. The derivative of the filtered phase jitter is used to test that $t_{SSC\text{-}FREQ\text{-}DEVIATION}$ meets the USB 3.2 specification for each SSC cycle must comply with +300/-300 and -3700/-5300 PPM

If the DUT is Type-C is x1 capable repeat all testing with the alternate Tx path by changing the CC state or by flipping the fixture. If Type-C is x2 capable, repeat all testing with other lane Tx without changing CC state.

Spec References

- USB 3.2 Specification, revision 1.1
    - Table 6-17, Figure 6-16
    - Table 6-18

3.5 Gen1 Clock Switch (BLR Retimers Port only)

This test verifies that the transmitter meets SSC profile requirements during clock switching operation when measured at the compliance test port. To comprehend noise effects, such as crosstalk, it is up to the DUT manufacturer to make sure that any other links are active for the various DUT types. Note: A PCI Express host adaptor is tested in a system that provides a 100 MHz PCI Express reference clock with a valid SSC profile and in a system with a 100 MHz PCI Express reference clock that does not have SSC. The host adaptor must pass all tests in both cases. No transmitter testing is done with multiple downstream ports active on hosts/hubs.

Overview of Test Steps

The test runs in the normal link training flow target state U0 and comprises of the following steps:

1. Connect the DUT to a simple break-out test fixture without VBUS supplied.
2. Connect BERT output to simple break-out test fixture Rx

Note: If the BERT is protocol aware it is allowed to just follow the protocol rules in the base specification

3. BERT sends either of the following sequences:
    i. Gen2 link flow
        1. 2-32 SCD1
        2. 2-32 SCD2
        3. 4-32 LBPM (w PHY capability set to Gen1x1).
        4. 4-32 LBPM (w PHY ready)
        5. Except typical SSC configuration all other jitter sources are disabled during all transmissions to the device under test.
        6. Transmit 65,536 TSEQ It is preferred for the BERT to transmit as close to 65,536 TSEQ as possible. If a device requires several TSEQ outside this range to pass the test this is a failure.
        7. Transmit 256 – 65,536 TS1. (SYNC, 31 TS1, SKP – repeat to up to 65,536 total TS1)
        8. Transmit 256 – 65,536 TS2 **w/o** Loopback (bit 2) or Bit-level re-timer Tx compliance (bit 5) bits asserted in the link configuration field (Table 6-6 in the USB3.2 specification).
    ii. Gen1 link flow
        1. 400 Polling.LFPS (4ms)
        2. 65,536 TSEQ
        3. 256-65,536 TS1
        4. 256-65,536 TS2 **w/o** Loopback (bit 2) or Bit-level re-timer Tx compliance (bit 5) bits asserted in the link configuration field

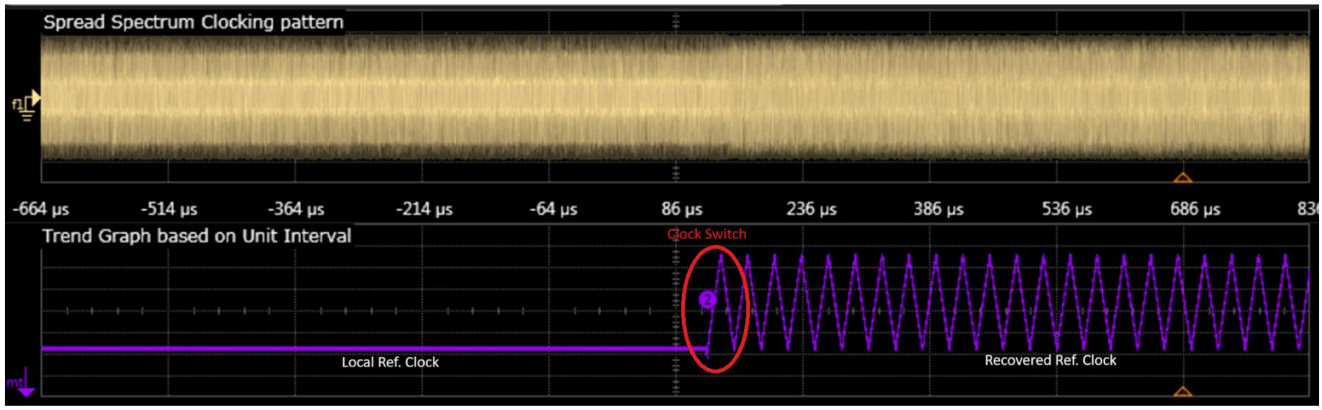
4. Power on the device under test and apply VBUS if the DUT is not a host, let it pass through the Rx.Detect state to the Polling.Idle state
5. Capture clock switching point waveform on the port under test and on a high-speed oscilloscope over a minimum of 2,000,000 unit intervals (400 μsec) at a sample rate of no more than 25 ps in a single scope capture. At least 5 SSC cycles must be preset in capture waveform post clock switching point.
6. Compute the phase jitter for the captured waveform and apply a 60*33KHz 3 dB cutoff frequency, 40 dB/decade Low Pass Filter to the phase jitter.
7. Use the filtered phase jitter to check that the SSC fundamental frequency is between 30 and 33 KHz.
8. Take the derivative of the filtered phase jitter and convert to ppm.
9. Check that switch point is compliant with the defined profile in USB3.2 base specification Table E-3 and Figure E-10

If the DUT is Type-C repeat all testing with the alternate Tx path by changing the CC state or by flipping the fixture.

Spec References

- USB 3.2 Specification, revision 1.1
  - Table E-3, Figure E-10
  - Table 6-18

➢ Scope capture example of the CLK SW event to be analyzed



3.6 Gen1 Jitter Transfer Function (JTF) (Component BLR Retimers only)

This test verifies that the transmitter meets Jitter Transfer Function (JTF) requirements as detailed in USB3.2 base specification. The test applies to Component level Retimers only and requires pattern control of both Retimer ports.

Overview of Test Steps

The test runs in the Loopback substate (Passthrough as introduced for Retimers) and performs the following steps.

1. Perform setup calibration:
    a. Connect BERT output to 1st simple breakout fixture (Plug/Rec.) Rx
    b. Connect 2nd simple breakout fixture (Rec./Plug) Tx to High-Speed Oscilloscope
    c. Connect both fixtures creating a path between BERT and Oscilloscope
    d. BERT Amplitude and equalization should be set to typical value
    e. All BERT signal stress component, jitter, SSC are disabled except single tone Pj
    f. Transmit the CP0 compliance pattern on the port under test and capture the transmitted waveform on a high-speed oscilloscope over a minimum of 1,000,000 unit intervals (200 μsec) at a sample rate of no more than 25 ps in a single scope capture.
    g. Adjust BERT Pj and capture waveforms per below 16 frequency/amplitude pairs:

Pj Freq.[KHz]	Pj Amp.[UI]
10,15,20,30,50	50
100,150,200,250,300,350	3
400,450,500,550,600	2

Table 3 - Tx Gen1 JTF profile

2. Connect the DUT ports to both simple break-out test fixtures without VBUS supplied.

Note: If the BERT is protocol aware it is allowed to just follow the protocol rules in the base specification

3. BERT sends either of the following sequences:
    i. Gen2 link flow
        1. 2-32 SCD1
        2. 2-32 SCD2
        3. 4-32 LBPM (w PHY capability set to Gen1x1).
        4. 4-32 LBPM (w PHY ready)

5. Transmit 65,536 TSEQ It is preferred for the BERT to transmit as close to 65,536 TSEQ as possible. If a device requires several TSEQ outside this range to pass the test this is a failure.
6. Transmit 256 – 65,536 TS1. (SYNC, 31 TS1, SKP – repeat to up to 65,536 total TS1)
7. Transmit 256 – 65,536 TS2 with Loopback (bit 2) asserted in the link configuration field (Table 6-6 in the USB3.2 specification).

ii. Gen1 link flow

1. 400 Polling.LFPS (4ms)
2. 65,536 TSEQ
3. 256-65,536 TS1
4. 256-65,536 TS2 with Loopback (bit 2) asserted in the link configuration field

4. Power on the device under test and apply VBUS if the DUT is not a host, let it pass through the Rx.Detect state to the Pass-Through Loopback State.
    - If the device does not go into Passthrough Loopback, it fails the test.
5. Transmit the CP0 compliance pattern on the port under test and capture the transmitted waveform on a high-speed oscilloscope over a minimum of 1,000,000 unit intervals (200 μsec) at a sample rate of no more than 25 ps in a single scope capture.
6. Adjust BERT Pj and capture waveforms per Table 3 frequency/amplitude pairs:
7. Analyze captured DUT waveform with respect to calibrated waveforms verifying compliance to USB3.2 base specification JTF Figure E-17 and Table E-4

If the DUT is Type-C repeat all testing with the alternate Tx path by changing the CC state or by flipping the fixture.

Spec References

- USB 3.2 Specification, revision 1.1
    - Table E-4, Figure E-17

3.7 Gen1x2 Lane to Lane Skew (Informative)

This test verifies that the transmitter meets Lane to Lane skew USB3.2 base specification requirements for x2 operation.

Overview of Test Steps

The test runs in the Polling.Compliance and performs the following steps.

1. Connect both lanes of the DUT to a simple break-out test fixture without VBUS supplied.
2. If the DUT is a host or a hub (for testing downstream ports) then run xHSETT and put the host/downstream hub port into compliance mode.
3. Power on the device under test and apply VBUS if the DUT is not a host, let it pass through the Rx.Detect state to the Polling.Compliance.
4. Transmit the CP0 compliance pattern on both lanes of the port under test.
5. Send PING.LFPS to the RX port configuration lane of the device under test to cause the compliance pattern promotion until is reached. A single PING.LFPS burst is sent with the following parameters:
    a. 100 nanosecond duration.
    b. 20 MHz frequency (2 periods).
6. Transmit the CP4 compliance pattern on both lanes of the port under test and capture the transmitted waveforms on a high-speed oscilloscope over a minimum of 1,000,000 unit intervals (200 μsec) at a sample rate of no more than 25 ps in a single scope capture.
7. Align both waveforms and report worst edge to edge skew between lanes.
8. Check compliance with respect to the below test point requirements:

Test Point	Max Skew (ps)	Description
TP2	2000	Tx Product Output/Cable Input
TP3	4600	Cable Output/Rx Product Input

Table 4 - Tx Gen1 Lane-to-Lane Skew Limits

Spec References

- USB 3.2 Specification, revision 1.1
    - Table 6-34, Figure 6-6

3.8 Gen2 Data Eye and Jitter

This test verifies that the transmitter meets the eye width, eye height, deterministic jitter and random jitter requirements when measured at the compliance test port with nominal transmitter equalization and after processing with the appropriate channels and post processing as shown in Table 5.

Connector Type	Channel	Reference Equalizer
Std-A	Device Under Test >> USB 3.2 Host Fixture 1A >> SCOPE (Embed 6dB Cable + Device PCB) SSGen2_TxComp12p2dB_Embedding.s4p	Long Channel
Micro-B	Device Under Test >> USB 3.2 Device Fixture 1A >> SCOPE (Embed 6dB Cable + Host PCB) SSGen2_TxComp12p2dB_Embedding.s4p	Long Channel
Type-C (Host)	Device Under Test >> USB 3.2 Host Fixture 1C >> SCOPE (Embed 6dB Cable + Host/Device PCB) SSGen2_TxComp12p2dB_Embedding.s4p	Long Channel
Type-C (Device)	Device Under Test >> USB 3.2 Device Fixture 1C >> SCOPE (Embed 6dB Cable + Host/Device PCB) SSGen2_TxComp12p2dB_Embedding.s4p	Long Channel
Captive (Standard A Plug)	Device Under Test >> USB 3.2 Captive Cable Device Fixture Type-A >> SCOPE (Embed Host PCB) Mock_Host_Cascaded_Model_TypeC_rspl.s4p	Long Channel
Captive (Standard C Plug)	Device Under Test >> USB 3.2 Captive Device Fixture Type-C >> SCOPE (Embed Host PCB) SSGen2_TxComp6p5dB_Embedding.s4p	Long Channel
All Types (except Captive C)	No Channel (USB3.2 Break-out fixture only)	Short Channel
Captive (Type C Plug)	No Channel (USB 3.2 Captive Device Fixture Type-C)	Short Channel

Table 5 - Tx Gen2 Channels and Reference Equalizer for Testing Device Types

Note: For connection topologies refer to
https://www.usb.org/sites/default/files/documents/usb3p1_fixture_topologies_11-8-2017_0.pdf
https://fixturesolution.com/wp-content/uploads/2025/01/FS-USB3.2-Gen2-Test-Topologies-V2.1.pdf

Note: Refer to https://www.usb.org/document-library/usb-32-embedding-files
For S-parameter files used for embedding the long channels when using breakout fixtures.
To comprehend noise effects, such as crosstalk, it is up to the DUT manufacturer to make sure that any other links are active for the various DUT types.
Note: Refer to Appendix 1 for the reference equalizer methodology.

Overview of Test Steps

The test runs in the Polling.Compliance substate and performs the following steps.

1. Connect the DUT to a simple break-out test fixture without VBUS supplied.
2. Power on the device under test and apply VBUS if the DUT is a device, let it pass through the Rx.Detect state to the Compliance state. SSC shall be enabled.
3. If the DUT is a host or a hub (for testing downstream ports) then run xHSETT and put the host/downstream hub port into compliance mode.
4. Send multiple PING.LFPS to the RX port of the device under test to cause the compliance pattern to transition to CP9. PING.LFPS bursts are sent with the following parameters:
    a. 100 nanosecond duration.
    b. 20 MHz frequency (2 periods).
5. If the DUT is x2 capable – both lanes must transmit same compliance patterns and promote in sync. When PING.LFPS is applied to configuration lane Rx
6. Transmit the CP9 compliance pattern on the Enhanced SuperSpeed USB port under test and capture the transmitted waveform on a high speed oscilloscope over a minimum of 2,000,000 unit intervals (200 μsec) at a sample rate of no more than 12.5 ps (no interpolation is used) in a single scope capture.
7. Send a PING.LFPS to the RX port of the device under test (for x2 capable apply to configuration lane only) to cause the compliance pattern to transition to CP10. A single PING.LFPS burst is sent with the following parameters:
    a. 100 nanosecond duration.
    b. 20 MHz frequency (2 periods).
8. Transmit the CP10 compliance pattern on the SuperSpeed USB port under test and capture the transmitted waveform on a high speed oscilloscope over a minimum of 2,000,000 unit intervals (200 μsec) at a sample rate of no more than 12.5 ps in a single scope capture.

The required compliance channel shown in Table 5 for the connector type under test is embedded to the measured CP9 data. No embedding is done for the short channel case.

The following analysis in steps 9-10 is done applying the reference equalizer shown in Table 5 and Appendix 1, and JTF (elaborated at Appendix 2) in the waveform analysis.

9. Compute Rj using the CP10 data and compare it against the normative transmitter specifications contained in the USB 3.2 specification (the equalizer is not applied for this step).

10. Compute the data eye using CP9 using Rj as input from the CP10 waveform and compare it against requirements for a 70 mV eye height and a 48.0 ps eye width both at 10^{-6} BER.

11. Repeat the analysis in steps 9-10 for the short channel shown in Table 5.

If the DUT is Type-C is x1 capable, repeat all testing with the alternate Tx path by changing the CC state or by flipping the fixture. If Type-C is x2 capable, repeat all testing with other lane Tx without changing CC state.

Spec References

- USB 3.2 Specification, revision 1.1
    - Table 6-20, Figure 6-20
    - Figure 6-17

3.9 Gen2 Spread Spectrum Clocking (SSC)

This test verifies that the transmitter meets SSC profile requirements when measured at the compliance test port with spec required TX equalization. To comprehend noise effects, such as crosstalk, it is up to the DUT manufacturer to make sure that any other links are active for the various DUT types.
Note: A PCI Express host adaptor is tested in a system that provides a 100 MHz PCI Express reference clock with a valid SSC profile and in a system with a 100 MHz PCI Express reference clock that does not have SSC. The host adaptor must pass all tests in both cases. No transmitter testing is done with multiple downstream ports active on hosts/hubs.

Overview of Test Steps

The test runs in the Polling.Compliance substate and performs the following steps.

1. Connect the DUT to a simple break-out test fixture without VBUS supplied.
2. If the DUT is a host or a hub (for testing downstream ports) then run xHSETT and put the host/downstream hub port into compliance mode.
3. Power on the device under test and apply VBUS if the DUT is not a host, let it pass through the Rx.Detect state to the Polling.Compliance
4. If the DUT is x2 capable – both lanes must transmit same compliance patterns and promote in sync. When PING.LFPS is applied to configuration lane Rx
5. Transmit the CP0 compliance pattern on the port under test.
6. Promote compliance patterns by sending a PING.LFPS to the RX port of the device under test (for x2 capable apply to configuration lane only) to cause the compliance pattern to transition to CP10. A single PING.LFPS burst is sent with the following parameters:
    a. 100 nanosecond duration.
    b. 20 MHz frequency (2 periods).
7. Transmit the CP10 compliance pattern on the port under test and capture the transmitted waveform on a high-speed oscilloscope over a minimum of 2,000,000 unit intervals (200 μsec) at a sample rate of no more than 12.5 ps in a single scope capture.
8. Compute the phase jitter for the captured waveform and apply a 60*33KHz 3 dB cutoff frequency, 40 dB/decade Low Pass Filter to the phase jitter.
9. Use the filtered phase jitter to check that the SSC fundamental frequency is between 30 and 33 KHz.
10. Take the derivative of the filtered phase jitter and convert to ppm.
11. Check that twice maximum difference between points that are 0.5 μs apart in the derivative of the filtered phase jitter is less than 1250 ppm.
12. The derivative of the filtered phase jitter is used to test that $t_{SSC\text{-}FREQ\text{-}DEVIATION}$ meets the USB 3.2 specification for each SSC cycle must comply with +300/-300 and -3700/-5300 PPM

If the DUT is Type-C is x1 capable repeat all testing with the alternate Tx path by changing the CC state or by flipping the fixture. If Type-C is x2 capable, repeat all testing with other lane Tx without changing CC state.

Spec References

- USB 3.2 Specification, revision 1.1
    - Table 6-17, Figure 6-16
    - Table 6-18

3.10 Gen2 Equalization

This test verifies that the transmitter meets requirements for transmit equalization. To comprehend noise effects, such as crosstalk, it is up to the DUT manufacturer to make sure that any other links are active for the various DUT types.

Note: A PCI Express host adaptor is tested in a system that provides a 100 MHz PCI Express reference clock with a valid SSC profile.

Overview of Test Steps

The test runs in the Polling.Compliance substate and performs the following steps.

1. Connect the DUT to a simple break-out test fixture without VBUS supplied.
2. If the DUT is a host or a hub (for testing downstream ports) then run xHSETT and put the host/downstream hub port into compliance mode.
3. Power on the device under test and apply VBUS if the DUT is not a host, let it pass through the Rx.Detect state to the Polling.Compliance or BLR Compliance state.
4. If the DUT is x2 capable – both lanes must transmit same compliance patterns and promote in sync. When PING.LFPS is applied to configuration lane Rx
5. Transmit the CP0 compliance pattern on the port under test.
6. Promote compliance patterns by sending a PING.LFPS to the RX port of the device under test (for x2 capable apply to configuration lane only) to cause the compliance pattern to transition to CP13. A single PING.LFPS burst is sent with the following parameters:
    a. 100 nanosecond duration.
    b. 20 MHz frequency (2 periods).
7. Transmit the CP13 compliance pattern on the port under test and capture the transmitted waveform on a high-speed oscilloscope over a minimum of 2,000,000 unit intervals (200 µs) at a sample interval of no more than 12.5 ps in a single scope capture.
8. Repeat steps 6 and 7 to capture transmitted waveforms for the CP14 and CP15 compliance patterns.
9. Use the SigTest Transmitter Equalization test option to read the saved waveform files for CP13, CP14, and CP15 and compute the transmitter equalization values from these. All transmitter equalization values must be within their specified limits.

If the DUT is Type-C is x1 capable repeat all testing with the alternate Tx path by changing the CC state or by flipping the fixture. If Type-C is x2 capable, repeat all testing with other lane Tx without changing CC state.

Spec References

- USB 3.2 Specification, revision 1.1
    - Table 6-21, Figure 6-23, Figure 6-24, Figure 6-25

3.11 Gen2x2 Lane to Lane Skew (Informative)

This test verifies that the transmitter meets Lane to Lane skew USB3.2 base specification requirements for x2 operation.

Overview of Test Steps

The test runs in the Polling.Compliance and performs the following steps.

1. Connect both lanes of the DUT to a simple break-out test fixture without VBUS supplied.
2. If the DUT is a host or a hub (for testing downstream ports) then run xHSETT and put the host/downstream hub port into compliance mode.
3. Power on the device under test and apply VBUS if the DUT is not a host, let it pass through the Rx.Detect state to the Polling.Compliance.
4. Transmit the CP0 compliance pattern on both lanes of the port under.
5. Send PING.LFPS to the RX port configuration lane of the device under test to cause the compliance pattern promotion until CP12 is reached. A single PING.LFPS burst is sent with the following parameters:
    a. 100 nanosecond duration.
    b. 20 MHz frequency (2 periods).
6. Transmit the CP12 compliance pattern on both lanes of the port under test and capture the transmitted waveforms on a high-speed oscilloscope over a minimum of 2,000,000 unit intervals (200 μsec) at a sample rate of no more than 12.5 ps in a single scope capture.
7. Align both waveforms and report worst edge to edge skew between lanes.
8. Check compliance with respect to the below test point requirements:

Test Point	Max Skew (ps)	Description
TP2	2000	Tx Product Output/Cable Input
TP3	4600	Cable Output/Rx Product Input

Table 6 - Tx Gen2 Lane-To-Lane Skew Limits

Spec References

- USB 3.2 Specification, revision 1.1
    - Table 6-34, Figure 6-6

4 Receiver Testing

Receiver compliance testing is defined at the input of connector facing receiver, TP3Ri for Retimer embedded systems and TP4 for non-Retimer systems. Both shortest possible case and worst-case channel loss are tested.

The following sections provide detailed information on the setup and testing of the USB3.2 parameters. In the event of a discrepancy, the USB3.2 Specification prevails.

Table 7 - Rx USB3.2 Electrical Compliance Test Points Definition

Test Point (TP)	Description
TP1	Transmitter silicon pad
TP2	Transmitter port connector mid-point
TP3	Receiver port connector mid-point
TP4	Receiver silicon pad
TP1Ro, TP3Ro	Re-timer transmitter silicon pad
TP1Ri, TP3Ri	Re-timer receiver silicon pad

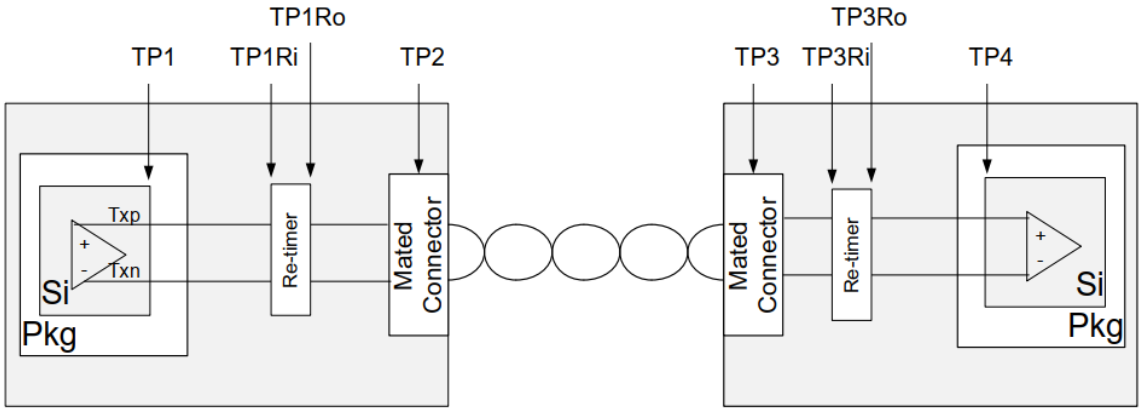


Figure 2 Rx USB3.2 Electrical Compliance Test Points Definition

4.1 Gen1 Low Frequency Periodic Signaling (LFPS) Sensitivity

This test verifies that the DUT low frequency periodic signal receiver recognizes LFPS signaling with voltage swings and duty cycles that are at the limits of what the specification allows. The link test specification includes test that vary additional LFPS parameters to test the LFPS receiver.

Overview of Test Steps

The test performs the following steps.

1. Connect the DUT to a simple breakout test fixture. Disconnect bus power if the DUT is a bus powered device.
2. Power on the device under test (connect bus powered if DUT is a bus powered device) and let it pass through the Rx.Detect state to the Polling.LFPS substate.
3. Trigger on the initial LFPS burst sent by the DUT and send LFPS signals to the DUT with the following parameters:
    a. tPeriod 50 ns.
    b. $V_{TX-DIFF-PP-LFPS}$ 800 mV.
    c. Duty Cycle 50%
4. The test passes if the device recognizes the LFPS and starts sending the TXEQ sequence following initial LFPS without reverting to Electrical Idle and new LFPS cycle.
5. The test is repeated with the following parameters:
    a. tPeriod 50 ns, $V_{TX-DIFF-PP-LFPS}$ 1200 mV, Duty Cycle 50%.
    b. tPeriod 50 ns, $V_{TX-DIFF-PP-LFPS}$ 1000 mV, Duty Cycle 40%.
    c. tPeriod 50 ns, $V_{TX-DIFF-PP-LFPS}$ 1000 mV, Duty Cycle 60%.
6. To verify Rx LFPS Detect Threshold ($V_{RX-LFPS-DET-DIFFp-p}$) (as specified in Table 6-22) the following test is performed:
    a. If the DUT reacts to voltages below "Min Spec" or does not react to voltages above "Max Spec" it would produce a result of fail.
7. Repeat steps 1 and 2 above
8. Trigger on the initial LFPS burst sent by the DUT and send LFPS signals to the DUT with the following parameters and register DUT response on scope:
    a. tPeriod 50 ns, $V_{RX-LFPS-DET-DIFFp-p}$ <= 100 mV, Duty Cycle 50%. **Normative – No Detect**
    b. tPeriod 50 ns, 100mv < $V_{RX-LFPS-DET-DIFFp-p}$ < 300 mV, Duty Cycle 50%. (**Informative**)
    c. tPeriod 50 ns, $V_{RX-LFPS-DET-DIFFp-p}$ >= 300 mV, Duty Cycle 50%. **Normative – Detect**

Spec References

- USB 3.2 Specification, revision 1.1
    - Table 6-22, Table 6-29

4.2 Gen2 SuperSpeedPlus Capability SCD and LBPM

This test verifies that the DUT low frequency periodic signal patterns SCD and LBPM are recognized by the receiver with voltage swings and duty cycles that are at the limits of what the specification allows.

Overview of Test Steps

The test performs the following steps.

1. Connect the DUT to a simple breakout test fixture. Disconnect bus power if the DUT is a bus powered device.
2. Connect DUT Rx lanes of the simple breakout fixture to signal generator transmitting repeating sequence of:
    a. 2-32 x SCD1
    b. 2-32 x SCD2
    c. 4-32 x LBPM with PHY Capability
    d. 4-32 x LBPM with PHY Ready
3. Power on the device under test (connect bus powered if DUT is a bus powered device) and let it pass through the Rx.Detect state to the Polling.LFPS substate.
4. Trigger on the initial LFPS burst sent by the DUT and send step 2 sequence signals to the DUT with the following parameters:
    a. tPeriod 50 ns.
    b. $V_{TX\text{-}DIFF\text{-}PP\text{-}LFPS}$ 800 mV.
    c. Duty Cycle 50%
5. The test passes if the device recognizes the SCD and LBPM sequence and starts sending the TXEQ following initial SCD and LBPM sequence without reverting to Electrical Idle and new LFPS cycle.
6. The test is repeated with the following parameters:
    a. tPeriod 50 ns, $V_{TX\text{-}DIFF\text{-}PP\text{-}LFPS}$ 1200 mV, Duty Cycle 50%.
    b. tPeriod 50 ns, $V_{TX\text{-}DIFF\text{-}PP\text{-}LFPS}$ 1000 mV, Duty Cycle 40%.
    c. tPeriod 50 ns, $V_{TX\text{-}DIFF\text{-}PP\text{-}LFPS}$ 1000 mV, Duty Cycle 60%.

Spec References

- USB 3.2 Specification, revision 1.1
    - Table 6-22, Table 6-29

4.3 Gen1x1 Receiver Jitter Tolerance (JTOL)

This test verifies that the receiver properly functions in the presence of deterministic and random jitter at multiple frequencies. The jitter characteristics are defined by the USB 3.2 specification. To reduce test time, the receiver is tested to a bit error ratio (BER) of 10^{-10}. To comprehend noise effects, such as crosstalk, it is up to the component manufacturer to make sure that any other links are active for the DUT.

The receiver test is performed with asynchronous SSC clocks in the test system and the device under test. The test system SSC shall be triangular at the maximum specified SSC frequency (33 kHz) and down spread 5,000 ppm. The test system SSC shall meet the specification limits on slew rate.

Note: When the DUT is in loopback for this test it shall not exit loopback unless it receives a warm reset or an LFPS Exit Handshake.

Connector Type	Calibration Channel (Using breakout fixture to measure at end of channel)	Test Channel
Std-A	3m Cable + 5" PCB	3m Cable + 5" PCB
Std-B	3m Cable + 11" PCB	3m Cable + 11" PCB
Micro-B	3m Cable + 11" PCB	1m Cable + 11" PCB
Tethered/Captive (Standard A Plug)	3m Cable + 11" PCB	8" (short) Std-A to Std-B cable + 11" PCB
Tethered/Captive (Type-C Plug)	BERT >> USB 3.2 Compliance Load Board Type-C >> 7 dB Cable >> USB 3.2 Device Fixture 1C >> USB 3.2 Mock Host/Device Type-C 7.2" >> SCOPE	BERT >> USB 3.2 Captive Device Fixture Type-C >> Device Under Test
All non-Type C Connectors Types Must Also Perform Short Channel Test	Same as above (Either 3m Cable + 5" PCB or 3m Cable + 11" PCB) depending on connector type	Breakout Fixture Only
Tethered/Captive device (Standard A-Plug) Must Also Perform Short Channel Test	Performed without the 3m cable, only 5" or 11" PCB used depending on the connector type	Breakout Fixture Only
Tethered/Captive device (Type C-Plug) Must Also Perform Short Channel Test	All calibration at BERT output	BERT -> USB3.2 Full Type-C Breakout -> DUT

Type-C (Host)	All calibration at BERT output	BERT -> 5G Host/Device Fixture 2 (14.4") -> 7 dB cable -> Host Fixture 1C -> DUT
Type-C (Device)	All calibration at BERT output	BERT -> 5G Host/Device Fixture 2 (14.4") -> 7 dB cable -> Device Fixture 1C -> DUT
Type-C Short Channel Test	All calibration at BERT output	BERT-> USB 3.2 Full Type-C Breakout -> DUT

Table 8 - Rx Gen1 Channels for Testing Device Types

Note: For connection topologies refer to https://www.usb.org/sites/default/files/documents/usb3p1_fixture_topologies_11-8-2017_0.pdf, https://www.usb.org/sites/default/files/documents/superspeedtesttopologies.pdf, https://fixturesolution.com/wp-content/uploads/2024/04/FS-USB3.2-Gen1-Test-Topologies.pdf

Overview of Test Steps

The test runs in the Loopback substate (Passthrough loopback for Retimers) and performs the following steps.

1. Calibrate swing and de-emphasis
    a. Connect the end of the cables that will connect to the SMAs on the test fixture (as directly as possible) to a real time oscilloscope and the other end to the test equipment generator.
    b. Have the test equipment transmit a pattern with 64 ones followed by 64 zeros followed by 128 bits of a 1010 clock pattern at 5 GT/s.
    c. Calibrate the differential amplitude of the measured signal to 800 mV peak to peak.
    d. Calibrate the measured de-emphasis to 3.0 + 0.3/-0 dB fixed de-emphasis.

Note: The signal source must support full bit de-emphasis.

2. Connect the calibration channel to the signal source.
    a. Calibrate Rj (2.42 +/- 10% ps RMS/30.8 +/- 10% ps peak to peak at a BER of 10^{-10}) with clock pattern (CP1). Calibrate at the end of the channel applying the CTLE and JTF. SSC and all other noise sources are off for this step.

    b. Calibrate Sj (40.0 ps +0/-10% at 50 MHz) with CP0. Calibrate at the end of the channel applying only CTLE. SSC is off for this step. (Calibration is done by testing measured maximum peak to peak jitter without extrapolation (measured TJ) without Sj and then adding Sj until measured maximum peak to peak jitter without extrapolation (measured Tj) increased by 40 ps).

All other noise sources are off during this calibration. A 49KHz critically damped high pass filter with 40 dB/decade roll-off is used during Sj calibration instead of the standard JTF.

3. If Non-Type C DUT is tested:

a. Measure eye height with CP0 at a BER E-6 at the end of the channel with the host fixtures with all jitter sources and SSC on applying the JTF and the Long channel reference CTLE. Adjust the signal source amplitude to provide

b. 180 mV +5/-0 mV of eye height with host test fixtures for testing a host.

c. 145 mV +5/-0 mV of eye height with device test fixtures for testing a device.

Note: Amplitude should be calibrated to be as close to the minimum value as possible without going under the minimum.

Note: De-emphasis at the instrument output must be adjusted to remain at 3.0 + 0.3/ - 0 dB after the eye height calibration process is complete.

d. After calibration is complete the Tj at a BER of 10^{-12} with CP0 and all jitter sources on must be between 90 and 95 picoseconds. This measurement is done only with the Sj frequency of 50 MHz and is performed by checking the average Tj over three 1-million-unit interval oscilloscope captures. Due to degradation in connections in the test channel or other test channel issues it may be necessary to switch to a new test channel to achieve a calibrated Tj value in the expected range.

4. Connect the calibration channel to the signal source.
5. Connect the DUT to the appropriate test channel.
6. Power on the device under test.
7. Transmit 400 Polling.LFPS (4ms).

   Note that all jitter sources are added during all transmissions to the device under test. If the device does not go into loopback, it fails the test.
8. Transmit 65,536 TSEQ.
9. Transmit 256-65,536 TS1.
10. Transmit 256-65,536 TS2 with Loopback bit set (bit 2 in the link configuration field Table 6-6 in the USB3.2 specification).
11. Start transmitting the BDAT test pattern.
12. Transmit BDAT for 2 ms before starting error calculations.
13. Transmit the BDAT sequence from the signal source for a total of $3x10^9$ symbols ($3x10^{10}$ bits). A single SKP ordered set is inserted in the sequence every 354 symbols.
14. The DUT fails If BERT detector receives more than a single K28.4 or 10b non-valid D0.0 symbol.

    Note: The channel to the test equipment receiver is kept as short and clean as possible.

15. Repeat steps 2b-14 with 40.0 +0/-10% ps of periodic (sinusoidal) at a 33 MHz frequency with -3dB of equalization.

16. Repeat steps 2b-14 with 40.0 +0/-10% ps of periodic (sinusoidal) at a 20 MHz frequency with -3dB of equalization.
17. Repeat steps 2b-14with 40.0 +0/-10% ps of periodic (sinusoidal) at a 10 MHz frequency with -3dB of equalization.
18. Repeat steps 2b-14 with 40.0 +0/-10% ps of periodic (sinusoidal) at a 4.9 MHz frequency with -3dB of equalization.
19. Repeat steps 2b-14 with 100 +0/-5% ps of periodic (sinusoidal) at a 2 MHz frequency with -3dB of equalization.
20. Repeat steps 2b-14 with 200 +0/-5% ps of periodic (sinusoidal) at a 1 MHz frequency -3dB of equalization.
21. Repeat steps 2b-14 with 400 +0/-5% ps of periodic (sinusoidal) at a 500 KHz frequency -3dB of equalization.

Connect scope directly to the signal source with the signal source keeping all settings the same as the calibrated settings with the calibration channel.

22. Measure the maximum peak to peak differential voltage with a pattern with 64 ones followed by 64 zeros followed by 128 bits of a 1010 clock pattern at 5 GT/s with all jitter sources, Tx Equalization, and SSC off. Adjust amplitude to provide a maximum peak to peak differential voltage of 1200 mV +0/-20 mV using the clock portion of the pattern for the measurement.
23. Turn all jitter sources, Tx Equalization and SSC on to the same settings as the long channel calibration and complete the short channel test with the DUT connected directly to the breakout fixture.

Note: Amplitude should be calibrated to be as close to the maximum value as possible without going over the maximum.
Note: De-emphasis at the instrument output must be adjusted to remain at 3.0 +0.3/-0 dB.

24. Repeat steps 3-21.

If the DUT is Type-C capable repeat all testing with the alternate Rx path by changing the CC state or by flipping the fixture.

4.4 Gen2x1 Receiver Jitter Tolerance (JTOL)

This test verifies that the receiver properly functions in the presence of deterministic and random jitter at multiple frequencies. The jitter characteristics are defined by the USB 3.2 specification. To comprehend noise effects, such as crosstalk, it is up to the component manufacturer to make sure that any other links are active for the DUT.
The receiver test is performed with asynchronous SSC clocks in the test system and the device under test. The test system SSC shall be triangular at the maximum specified SSC frequency (33KHz) and down spread 5,000 ppm. The test system SSC shall meet the specification limits on slew rate.
Note: When the DUT is in loopback for this test it shall not exit loopback unless it receives a warm reset or an LFPS Exit Handshake.

Note: The test procedures for channels involving a USB cable assume the cable is selected to have a well-controlled nominal loss of 6.0 dB at 5.0 GHz.

Connector Type	Calibration Channel (Using breakout fixture to measure at end of channel)	Test Channel
Std-A	BERT >> USB 3.2 Compliance Load Board >> 6 dB Cable >> USB 3.2 Host Fixture 1A >> USB 3.2 Mock Host 7.2" >> SCOPE	BERT >> USB 3.2 Compliance Load Board >> 6 dB Cable >> USB 3.2 Host Fixture 1A >> Host Under Test
Micro-B	BERT >> USB 3.2 Compliance Load Board >> 6 dB Cable >> USB 3.2 Device Fixture 1A >> USB 3.2 Mock Device 7.2" >> SCOPE	BERT >> USB 3.2 Compliance Load Board >> 6 dB Cable >> USB 3.2 Device Fixture 1A >> Device Under Test
Captive (Standard A Plug)	BERT >> USB 3.2 Compliance Load Board >> 6 dB Cable >> USB 3.2 Device Fixture 1A >> USB 3.2 Mock Device 7.2" >> SCOPE	BERT >> USB 3.2 Captive Cable Device Fixture Type-A >> Device Under Test
Type-C Host	BERT >> USB 3.2 Compliance Load Board Type–C >> 6 dB Cable >> USB 3.2 Host Fixture 1C >> USB 3.2 Mock Host/Device Type-C 7.2" >> SCOPE	BERT >> USB 3.2 Compliance Load Board Type–C >> 6 dB Cable >> USB 3.2 Host Fixture 1C >> Device Under Test
Type-C Device	BERT >> USB 3.2 Compliance Load Board Type–C >> 6 dB Cable >> USB 3.2 Device Fixture 1C >> USB 3.2 Mock Host/Device Type-C 7.2" >> SCOPE	BERT >> USB 3.2 Compliance Load Board Type–C >> 6 dB Cable >> USB 3.2 Device Fixture 1C >> Device Under Test

Captive (Type-C Plug)	BERT >> USB 3.2 Compliance Load Board Type–C >> 6 dB Cable >> USB 3.2 Device Fixture 1C >> USB 3.2 Mock Host/Device Type-C 7.2" >> SCOPE	BERT >> USB 3.2 Captive Device Fixture Type-C >> Device Under Test
All Connector Types Must Also Perform Short Channel Test	See procedure for short channel calibration details	For Type –C BERT>>USB 3.2 Full Type-C Breakout>>DUT For Standard A – Use breakout fixture from a test vendor used for 5 GT/s testing
Captive Device Must Also Perform Short Channel Test	At the end of the cable – TP2	For Type–C BERT>> USB3.2 Full Type-C Breakout >> DUT For Standard A – Use breakout fixture from a test vendor used for 5 GT/s testing

Table 9 - Rx Gen2 Channels for Testing Device Types

Note: For connection topologies refer to
https://www.usb.org/sites/default/files/documents/usb3p1_fixture_topologies_11-8-2017_0.pdf
https://fixturesolution.com/wp-content/uploads/2025/01/FS-USB3.2-Gen2-Test-Topologies-V2.1.pdf

Note: All cable losses in dB are at 5 GHz

Overview of Test Steps

The test runs in the Loopback substate (Pass-Through Loopback for Retimers) and performs the following steps.

1. Calibrate swing and de-emphasis without the test channel.
    a. Connect the end of the SMA cables that will connect to the SMAs on the test fixture (as directly as possible) to a real time oscilloscope and the other end to the test equipment generator.
    b. Have the test equipment transmit a pattern with 64 ones followed by 64 zeros followed by 128 bits of a 1010 clock pattern at 10 GT/s.
    c. Measure the transmitted signal on the oscilloscope and adjust the post cursor de-emphasis and swing of the generator until the low frequency and high frequency portions of the signal have an equal differential amplitude of 800 mV peak to peak.
    d. Calibrate the measured TX EQ to 2.2 +/- 1.0 dB fixed preshoot
    e. Calibrate the TX EQ de-emphasis settings for -1.0 +/- .1 dB, -3.1 +/- 1 dB, and -5.0 +/- .1 dB

Note: The signal source must support full bit de-emphasis.

2. Calibrate Rj (1.0 +0/-.1 ps RMS) with clock pattern (CP10). Calibrate after applying the JTF. The reference equalizer is not used for this Rj calibration. SSC is off and all other jitter sources are on but set to zero.

3. Calibrate Sj (17.0 ps +0/-10% at 100 MHz) with CP9. Calibrate without reference receiver equalization. SSC is off and all other jitter sources are on but set to zero. Calibration is done by testing measured maximum peak to peak jitter without extrapolation (measured TJ) without Sj and then adding Sj until measured maximum peak to peak jitter without extrapolation (measured Tj) increased by 17 ps. A 75KHz critically damped high pass filter with 40 dB/decade roll-off is used during Sj calibration instead of the standard JTF.

4. Connect the calibration channel to the signal source using the shortest compliance load board (5.6”).

5. Measure eye height with CP9 at a BER E-6 using the calibrated Sj and Rj values with SSC enabled. The eye height is measured after applying the JTF, the reference CTLE curve fixed to a DC gain of -5 dB, and DFE.

6. Change the compliance load board to the mid-length (7.1”) and repeat the eye height measurement.

7. Change the compliance load board to the longest (8.1”) and repeat the eye height measurement.

8. Select the compliance load board that yields the eye height measurement closest to 70 mV and use this compliance load board for the remaining calibration and testing.

9. Adjust the de-emphasis from 1 dB to 5 dB to adjust the eye width with a target of 48 +2/-0 ps. The width is measured after applying JTF, the reference equalizer CTLE curve fixed to a DC gain of -5 dB, and DFE. SSC is still enabled for this step.

10. If the width target was not met in step 10 then:
    a. If the width is too big then add a second Sj tone at 87 MHz and adjust until the width target is met.
    b. If the width is too small, then reduce the 100 MHz Sj tone until the width target is met.

Note: If the adjustment in step 10a or 10b is bigger than 5 ps then there is likely a problem with the fixtures or set-up.

11. Adjust the signal source amplitude to provide

    70 mV +5/-0 mV of eye height with calibration channel.
    Note: Amplitude should be calibrated to be as close to the minimum value as possible without going under the minimum.

12. Connect the DUT to the appropriate test channel.

13. Power on the device under test.

Note: If the BERT is protocol aware it is allowed to just follow the protocol rules in the base specification

14. BERT sends following sequences
    a. 2-32 SCD1
    b. 2-32 SCD2
    c. 4-32 LBPM (w PHY capability).
    d. 4-32 LBPM (w PHY ready)

    Note that all jitter sources are added during all transmissions to the device under test. If the device does not go into loopback, it fails the test.

15. Transmit 524,288 - 577,288 TSEQ It is preferred for the BERT to transmit as close to 524,288 TSEQ as possible. If a device requires several TSEQ outside this range to pass the test this is a failure.

16. Transmit 31 – 65,536 TS1. (SYNC, 31 TS1, SKP – repeat to up to 65,536 total TS1)
17. Transmit 31 – 65,536 TS2 with Loopback bit set (bit 2 in the link configuration field Table 6-6 in the USB3.2 specification).
18. Start transmitting the CP9 test pattern.
19. Transmit CP9 for 2 ms before starting error calculations.
20. Transmit a "modified" CP9 sequence from the signal source for a total of 2 minutes. The modified CP9 pattern starts with a SYNC ordered set. Then data blocks are added and scrambled with the USB10G specific PRBS-23 scrambler polynomial.

    A single SKP ordered set with 20SKP symbols (192 bits) must be inserted in the sequence every 40 blocks. At least 65,536 data blocks must be sent before the pattern is repeated.
21. The DUT fails if more than one error is encountered.

    Note: The channel to the test equipment receiver is kept as short and clean as possible.

    Note: if adjustments were made in step 10, they are kept for each additional Sj frequency. If an 87 MHz tone was used it is kept at the same magnitude for each Sj frequency. If the 100 MHz Sj tone was reduced the Sj targets at each other frequency is reduced by the same amount in ps.

22. Repeat steps 3,14-21 with 17.0 +0/-10% ps of periodic (sinusoidal) at a 50 MHz frequency.
23. Repeat steps 3,14-21 with 17.0 +0/-10% ps of periodic (sinusoidal) at a 30 MHz frequency.
24. Repeat steps 3,14-21 with 17.0 +0/-10% ps of periodic (sinusoidal) at a 15 MHz frequency.
25. Repeat steps 3,14-21 with 17.0 +0/-10% ps of periodic (sinusoidal) at a 7.5 MHz frequency.
26. Repeat steps 3,14-21 with 37.0 +0/-5% ps of periodic (sinusoidal) at a 4 MHz frequency.

27. Repeat steps 3,14-21 with 87.0 +0/-5% ps of periodic (sinusoidal) at a 2 MHz frequency.
28. Repeat steps 3,14-21 with 203.0 +0/-5% ps of periodic (sinusoidal) at a 1 MHz frequency.
29. Repeat steps 3,14-21 with 476.0 +0/-5% ps of periodic (sinusoidal) at a 500 KHz frequency.

Connect the scope directly to the signal source with the signal source keeping all settings the same as the calibrated settings with the calibration channel.

30. Measure the maximum peak to peak differential voltage with a pattern with 64 ones followed by 64 zeros followed by 128 bits of a 1010 clock pattern at 10 GT/s with all jitter sources, Tx Equalization, and SSC off. Adjust amplitude to provide a maximum peak to peak differential voltage of 1200 mV +0/-20 mV using the clock portion of the pattern for the measurement.

Note: Amplitude should be calibrated to be as close to the maximum value as possible without going over the maximum. TX EQ must not change during this calibration.

31. Turn all jitter sources, Tx Equalization, and SSC on to the same settings as the long channel calibration and complete the short channel test with the DUT connected directly to the breakout fixture.
32. Repeat steps 12-29

If the DUT is Type-C repeat all testing with the alternate Rx path by changing the CC state or by flipping the fixture. If the CC state is changed the eye calibration is repeated for the new fixture path.

Appendix 1 - Tx Compliance Reference Receiver Equalizer Functions

The normative transmitter eye is captured at the end of the reference channel. At this point the eye may be closed. To open the eye so it can be measured a reference Rx equalizer, is applied to the signal.

USB 3.2 allows the use of receiver equalization to meet system timing and voltage margins. For long cables and channels the eye at the Rx is closed, and there is no meaningful eye without first applying an equalization function. The Rx equalizer may be required to adapt to different channel losses using the Rx EQ training period. The exact Rx equalizer and training method is implementation specific.

The equation for the Gen1 reference continuous time linear equalizer (CTLE) used to develop the specification is the compliance Rx EQ transfer function described below

$$H(s) = \frac{A_{dc}\omega_{p1}\omega_{p2}}{\omega_z} \cdot \frac{s+\omega_z}{(s+\omega_{p1})(s+\omega_{p2})}$$

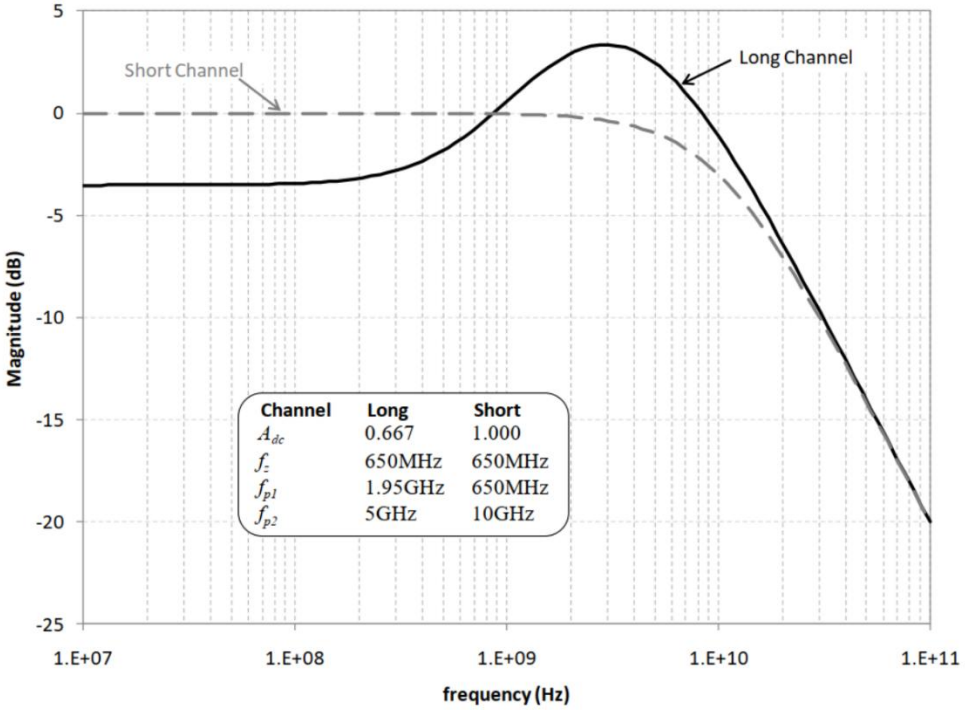
where A_{dc} is the DC gain

$\omega_z = 2\pi f_z$ is the zero frequency

$\omega_{p1} = 2\pi f_{p1}$ is the first pole frequency

$\omega_{p2} = 2\pi f_{p2}$ is the second pole frequency

Figure 6-27 is a plot of the Compliance EQ transfer functions with the values for each of the input parameters.



The equation describes the frequency response for the Gen2 reference continuous time linear equalizer (CTLE) that is used for compliance testing. The equation describes the same first order CTLE as contained in the Gen1 equation above.

$$H(s) = A_{ac}\omega_{p2}\frac{s + \frac{A_{dc}}{A_{ac}}\omega_{p1}}{(s+\omega_{p1})(s+\omega_{p2})}$$

where A_{ac} is the high frequency peak gain

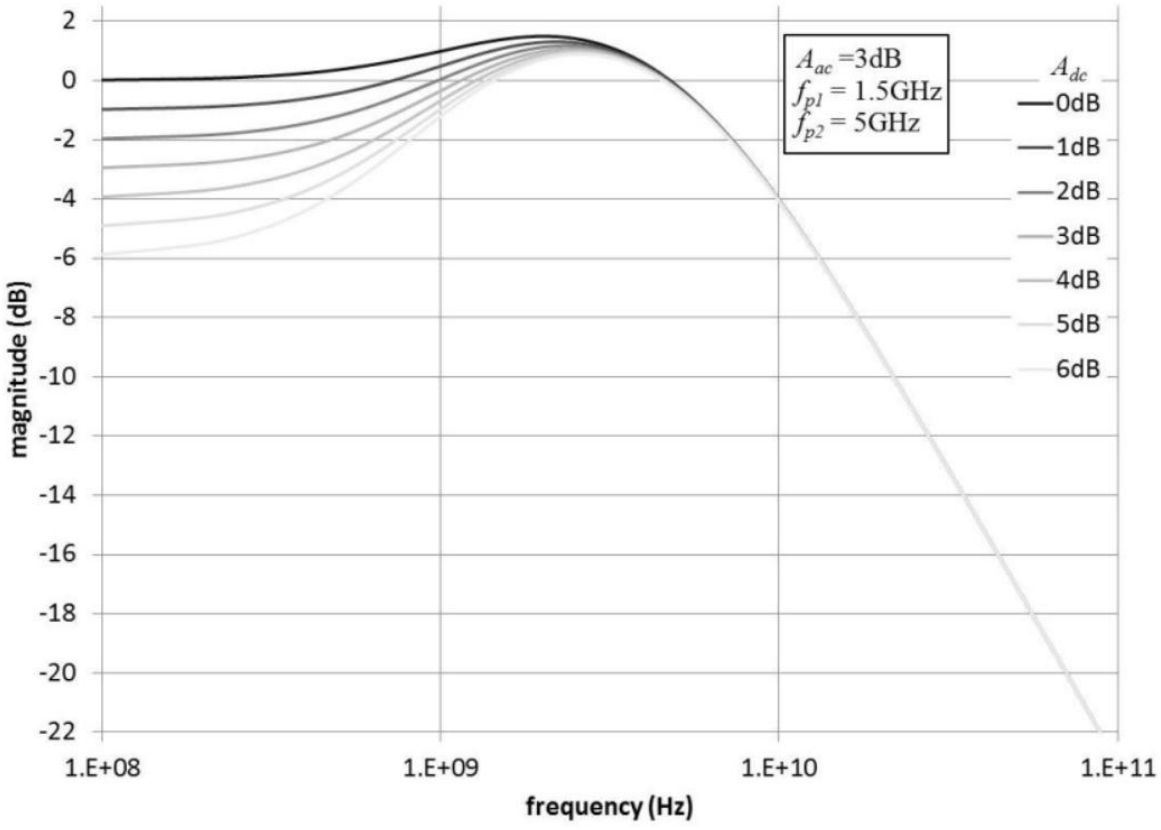
A_{dc} is the DC gain

$\omega_{p1} = 2\pi f_{p1}$ is the first pole frequency

$\omega_{p2} = 2\pi f_{p2}$ is the second pole frequency

Figure 6-28 is a plot of the Compliance EQ transfer functions with the values for each of the input parameters.

Figure 6-28. Gen 2 Compliance Rx EQ Transfer Function



In addition to the 1st order Gen2 CTLE, a one-tap reference DFE is used in transmitter compliance testing.
The DFE behavior is described by the equation below and Figure 6-29.
The limits on d1 tap are 0 to 50mV.

$$y_k = x_k - d_1 \operatorname{sgn}(y_{k-1})$$

where y_k is the DFE differential output voltage

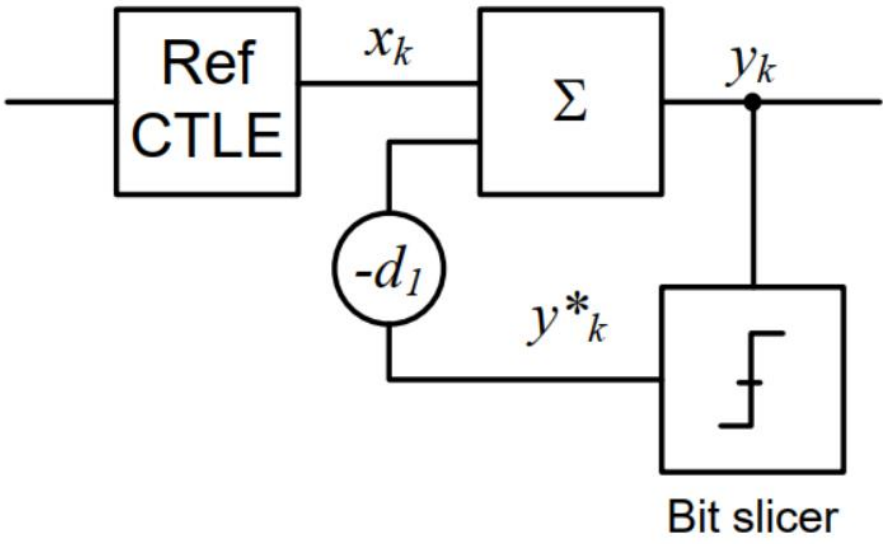
y^*_k is the decision function output voltage, $|y^*_k| = 1$

x_k is the DFE differential input voltage

d_1 is the DFE feedback coefficient

k is the sample index in UI

Figure 6-29. Gen 2 reference DFE Function



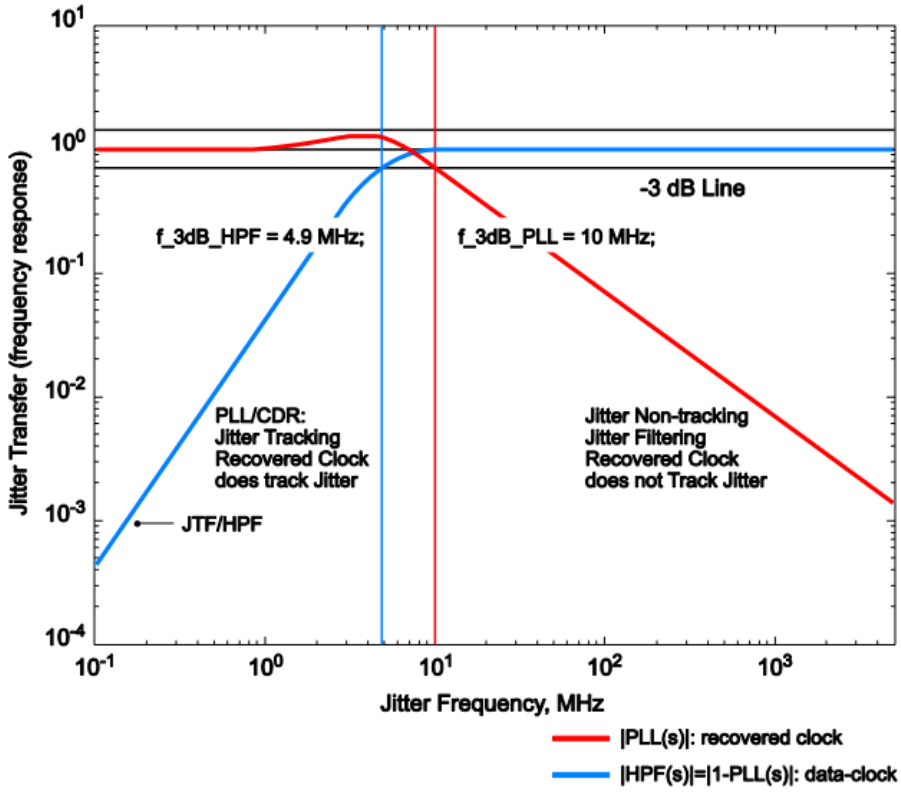
Spec References

- USB 3.2 Specification, revision 1.1
  - Section 6.8.2

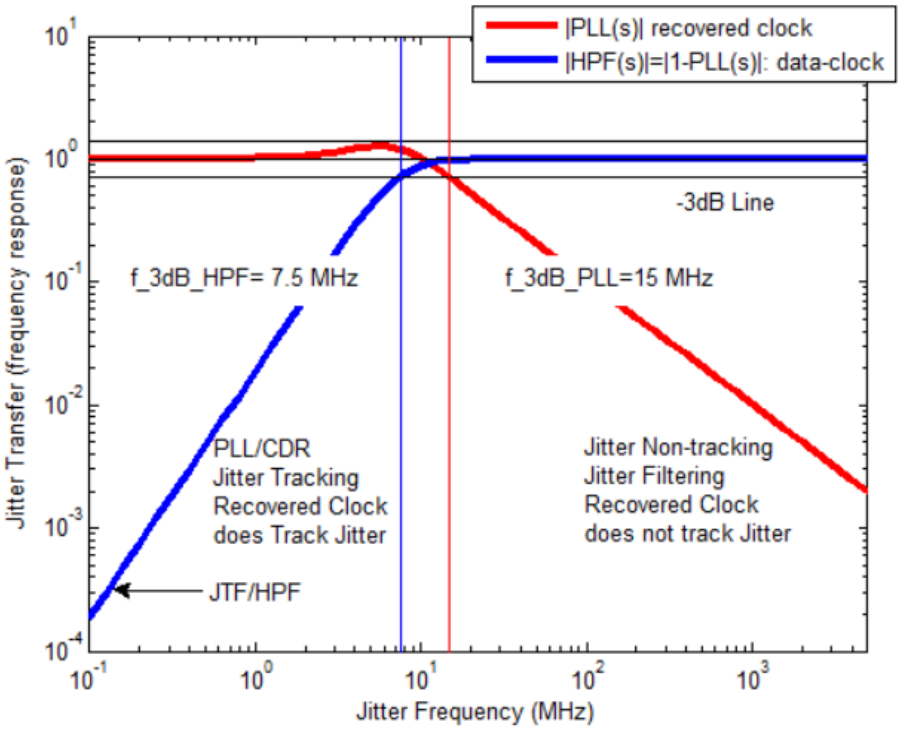
Appendix 2 - "Golden PLL" and Jitter Transfer Function

- JTF (Jitter Transfer Function) is used for clock recovery in the context of evaluating the performance of the transmitter under various jitter conditions.
- Tx is measured after application of the JTF as described in the figures below.
- The transfer function for the jitter suppression filter may be either first order or second order, depending upon implementation.

"Golden PLL" and Jitter Transfer Function for Gen1 operation



"Golden PLL" and Jitter Transfer Function for Gen2 operation

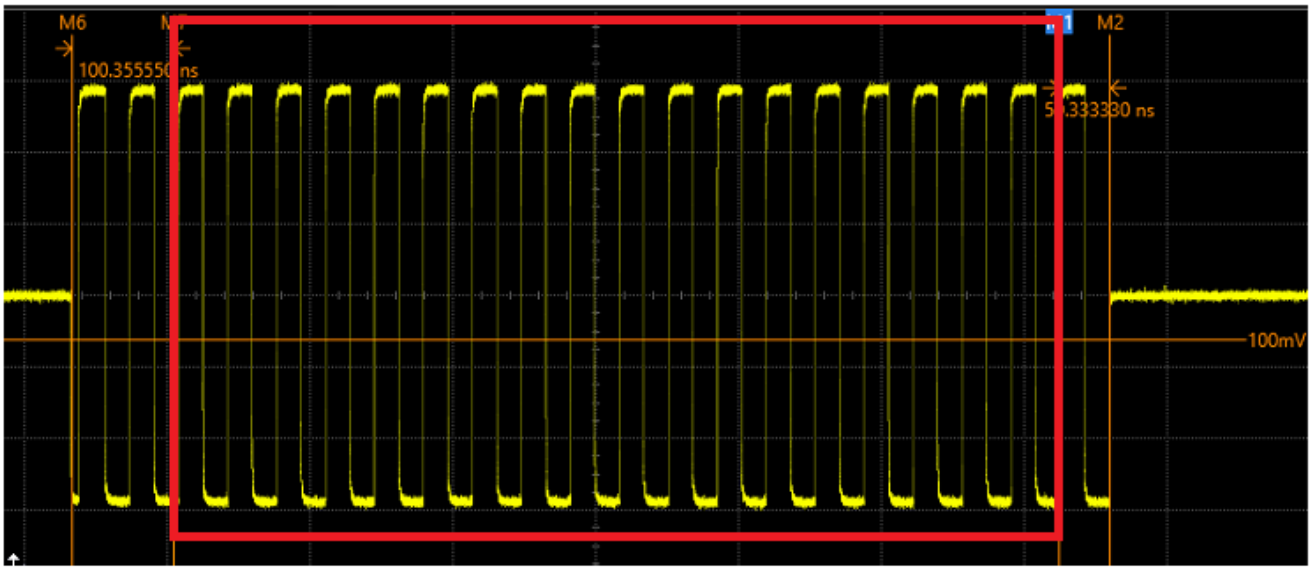


Spec References

- USB 3.2 Specification, revision 1.1
  - Section 6.5.2

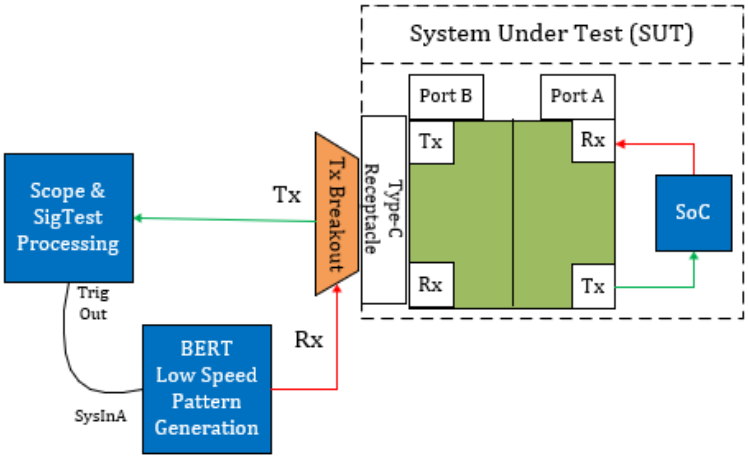
Appendix 3 - LFPS measurement zone definition for tPeriod, tRiseFall2080, Duty Cycle, VCM-AC-LFPS, and VTX-DIFF-PP-LFPS

- tPeriod, tRiseFall2080, Duty cycle, $V_{CM\text{-}AC\text{-}LFPS}$, and $V_{TX\text{-}DIFF\text{-}PP\text{-}LFPS}$ are only measured during the period from 100 nanoseconds after the burst start to 100 nanoseconds before the burst stop



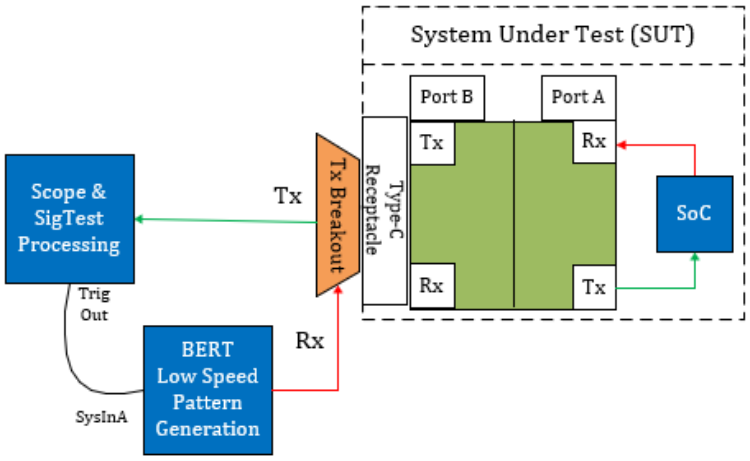
Appendix 4 - TX LFPS Gen1 Test methodology flow for an embedded Retimer system

- Power on DUT
- RxDetect (Scope and Analyzer/Rrx-dc terminations) -> Retimer mimic termination detect by exposing its Rx terminations
- SoC detecting Retimer Port A Rx termination -> expose its own Rx termination and start sending Low Speed signaling (SCD1 if USB3.1 mode SoC, or Polling.LFPS if USB3.0 mode SoC)
- BERT sending the following training sequence (Triggered by SCD1/Polling.LFPS forwarded from SoC via Retimer):
  - To Port B (Under Test): Polling.LFPS
- During link training the Retimer will respond as follows:
  - Forward SCD1/Polling.LFPS From Port A Rx (SoC side) to Port B Tx with local clock
  - Forward Polling.LFPS From Port B Rx (BERT side) to Port A Tx with local clock
  - USB3.1 SoC – once Polling.LFPS is received, it will stop sending SCD1 and transition to Polling.LFPS as part of Gen1 configuration (time to transition is design dependent)
  - USB3.0 SoC – Transmit Polling.LFPS from the begging of the link training sequence



Appendix 5 - TX LFPS Gen2 Test methodology flow for an embedded Retimer system

- Power on DUT
- RxDetect (Scope and Analyzer/Rrx-dc terminations) -> Retimer mimic termination detect by exposing its Rx terminations
- SoC detecting Retimer Port A Rx termination -> expose its own Rx termination and start sending Low Speed signaling (SCD1 since by default start at USB3.1 mode)
- BERT sending the following training sequence (Triggered by SCD1 forwarded from SoC via Retimer):
    - To Port B (Under Test): SCD1 -> SCD2 -> LBPM Capability -> LBPM Ready
- During link training the Retimer will respond as follows:
    - Forward SCD1/SCD2/LBPM From Port A Rx (SoC side) to Port B Tx with local clock
    - Forward SCD1/SCD2/LBPM From Port B Rx (BERT side) to Port A Tx with local clock



Appendix 6 - TX BLR compliance Test methodology flow for an embedded Retimer system

- Power on DUT
- RxDetect (Scope and Analyzer/Rrx-dc terminations) -> Retimer mimic termination detect by exposing its Rx terminations
- SoC detecting Retimer Port A Rx termination -> expose its own Rx termination and start sending Low Speed signaling (SCD1 if USB3.2/3.1 mode SoC, or Polling.LFPS if USB3.0 mode SoC)
- BERT sending the following training sequence (Triggered by SCD1/Polling.LFPS forwarded from SoC via Retimer):
    - To Port B (Under Test): Polling.LFPS -> TSEQ -> TS1 ->TS2 with link configuration field bits set to "BLR Compliance" and "Passthrough Loopback"
- During link training the Retimer will respond as follows:
    - Forward Polling.LFPS From Port B Rx (BERT side) to Port A Tx with local clock
    - Forward SCD1 (if USB3.2/3.1 SoC) or Polling.LFPS (if USB3.0 SoC) From Port A Rx (SoC side) to Port B Tx with local clock
    - SoC – once Polling.LFPS is received it will stop sending SCD1 and transition to Polling.LFPS as part of Gen1 configuration (time to transition is design dependent)
    - Transmit TSEQ at both ports with local clock without SSC and perform Rx EQ (both ports – BERT sending TSEQ to port B and SoC sending TSEQ to port A)
    - Once TSEQ is complete, transmit TS1A* (may not be captured if Retimer has quickly switched to other port Rx) -> SoC will ignore TS1A and not transition to TS2
    - Count 8 x TS1 at its Ports Rx (coming from BERT and SoC)
    - Perform clock switch -> both ports transmit TS1 with recovered clock -> SOC will now transition to TS2
    - Decode TS2 link configuration field -> BERT side will contain BLR Compliance + Passthrough loopback, SoC side will contain only Passthrough loopback since BLR compliance bit is ignored
    - Port B (Under Test) transition to BLR Compliance mode -> start transmitting CP0 (with recovered clock from Port A Rx)
    - Port A transition to Passthrough Loop back mode (pass data + clock from Port A Rx) -> BERT set jitter to 50MHz Calibrated Sj

Compliance patterns at the Retimer port are promoted by sending 4 x SKP OS from BERT between CP0 which is present to maintain Port A Rx lock

Note: Each Gen1 SKP Ordered Set consists of x2 SKP symbols (K28.1), meaning, for a single CP promotion x8 SKP symbols shall be sent (Refer to USB3.2 spec section E.3.6.1 and 6.4.3.1 for reference).

Table 6-12. Gen 1 SKP Ordered Set Structure

Symbol Number	Encoded Values	Description
0	K28.1	SKP
1	K28.1	SKP

- Scope capture example of the SKP symbol (K28.1)

Table A-2. 8b/10b Special Character Symbol Codes

Data Byte Name	Data Byte Value (hex)	Bits HGF EDCBA (binary)	Current RD– abcdei fghj (binary)	Current RD+ abcdei fghj (binary)
K28.1	3C	001 11100	001111 1001	110000 0110